REVISION HISTORY

Revision	Description	Date	Drawn	Checked
Ver 1.0	Initial Version	2023-12-29	HHY	
Ver 1.1	Initial Version	2024-01-31	HHY	

1、WIFI_SDIO修改
① WL-SDIO-D2-A&WL-SDIO-D3互换
2、LED灯状态修改（修改原理）
（1）PWR直接开机亮（R16原330R改为10K）
（2）SYS系统启动之后亮（R12/R15/Q3取消掉NC，R14原47K改为10K，R29原10K改为1K）
3、修改以太网
（1）VCCIO PHY0原1.8V芯片内部输出电压，现要求改为外部3.3V供电（RE37原10改为0R）
（2）增加RST复位IO口，原USB限流IC控制口兼容到PHY复位使用（新增RE14为0R贴片电阻）
4、修改USB
（1）修改USB限流IC原有IO口控制改用5V上拉不受控制（新增RU5为100K贴片电阻）
5、修改TF不读（通电之前插串口线）
（1）修改TF卡3.3V供电增加RC8/RC9=120R负载电阻放电
6、修改AV耳机插座
（1）修改AV耳机插座，将AV功能取消，改用K1版本一样的耳机插座

Schematics Index:

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Option
P15 DDR3 16X2
P16 DDR4 16X4
P17 WIFI BT XR829

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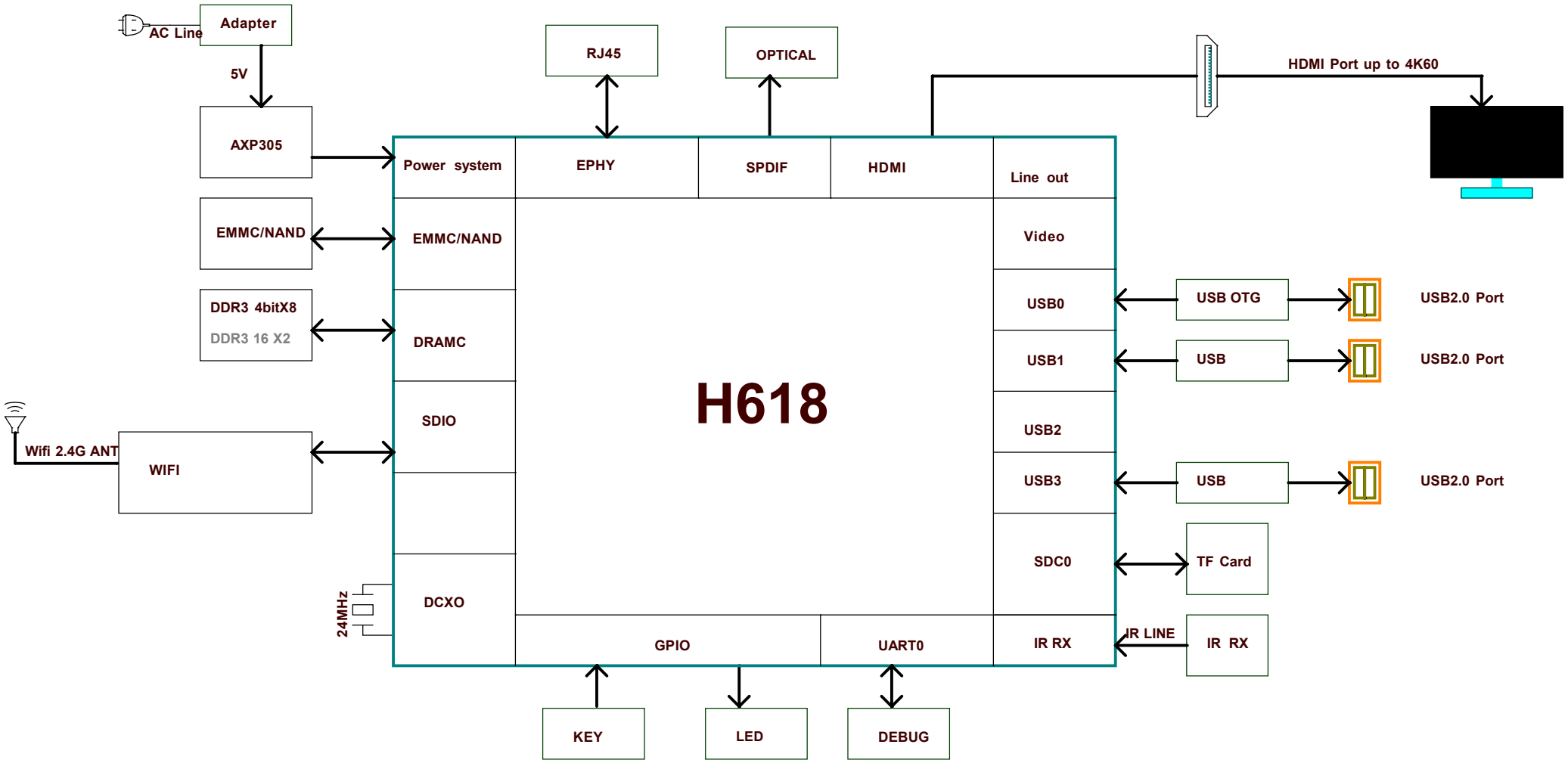
BLOCK



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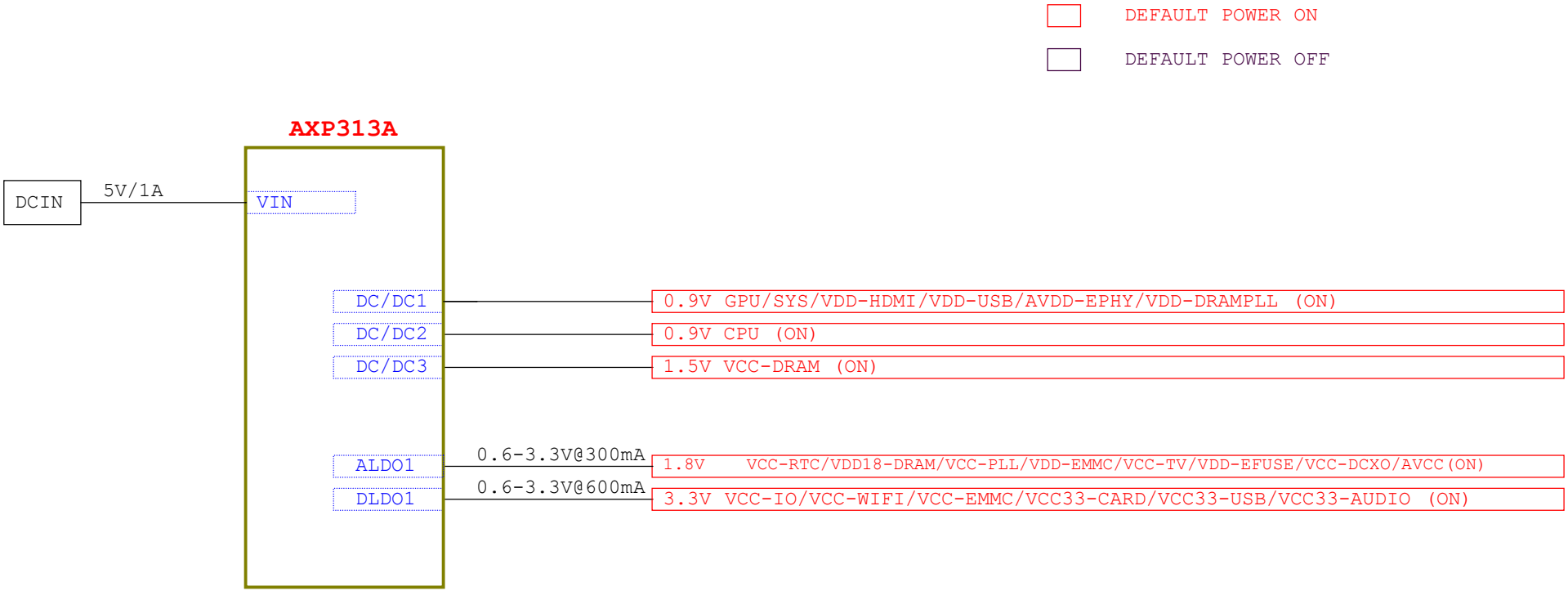
POWER TREE



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GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE/SDC2_DS	2/3	NAND/eMMC
PC1	NAND_ALE/SDC2_RST	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE1	2	
PC4	NAND_CE0	2	
PC5	NAND_RE/SDC2_CLK	2/3	
PC6	NAND_RB0/SDC2_CMD	2/3	
PC7	NAND_RB1	2	
PC8	NAND_DQ7/SDC2_D3	2/3	
PC9	NAND_DQ6/SDC2_D4	2/3	
PC10	NAND_DQ5/SDC2_D0	2/3	
PC11	NAND_DQ4/SDC2_D5	2/3	
PC12	NAND_DQS	2	
PC13	NAND_DQ3/SDC2_D1	2/3	
PC14	NAND_DQ2/SDC2_D6	2/3	
PC15	NAND_DQ1/SDC2_D2	2/3	
PC16	NAND_DQ0/SDC2_D7	2/3	

PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD0
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	WIFI+BT
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	
PG7	UART1_RX	2	
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	AP-CK32KO	3	
PG11	PCM2_SYNC	2	
PG12	PCM2_CLK	2	
PG13	PCM2_DOUT	2	
PG14	PCM2_DIN	2	
PG15	WL-WAKE-AP	0	
PG16	BT-WAKE-AP	0	
PG17	AP-WAKE-BT	1	
PG18	WL-REG-ON	1	
PG19	BT-REG-ON	1	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2	FD628-SCK	X	
PH3	FD628-SDA	X	
PH4	SPDIF-OUT	3	
PH5		1	
PH6	SYS-LED	1	
PH7		1	
PH8	USB0-DRVVBUS	1	
PH9	RECOVERY	0	
PH10	IR-RX	3	

X:Network port lights need to be configured

PIN	Define	CFG	Function
PI0			
PI1			
PI2			
PI3			
PI4			
PI5			
PI6			
PI7			
PI8			
PI9			
PI10			
PI11			
PI12			
PI13			
PI14			
PI15			
PI16			

PIN	Define	CFG	Function
PL0	PMU-SCK	2	
PL1	PMU-SDA	2	

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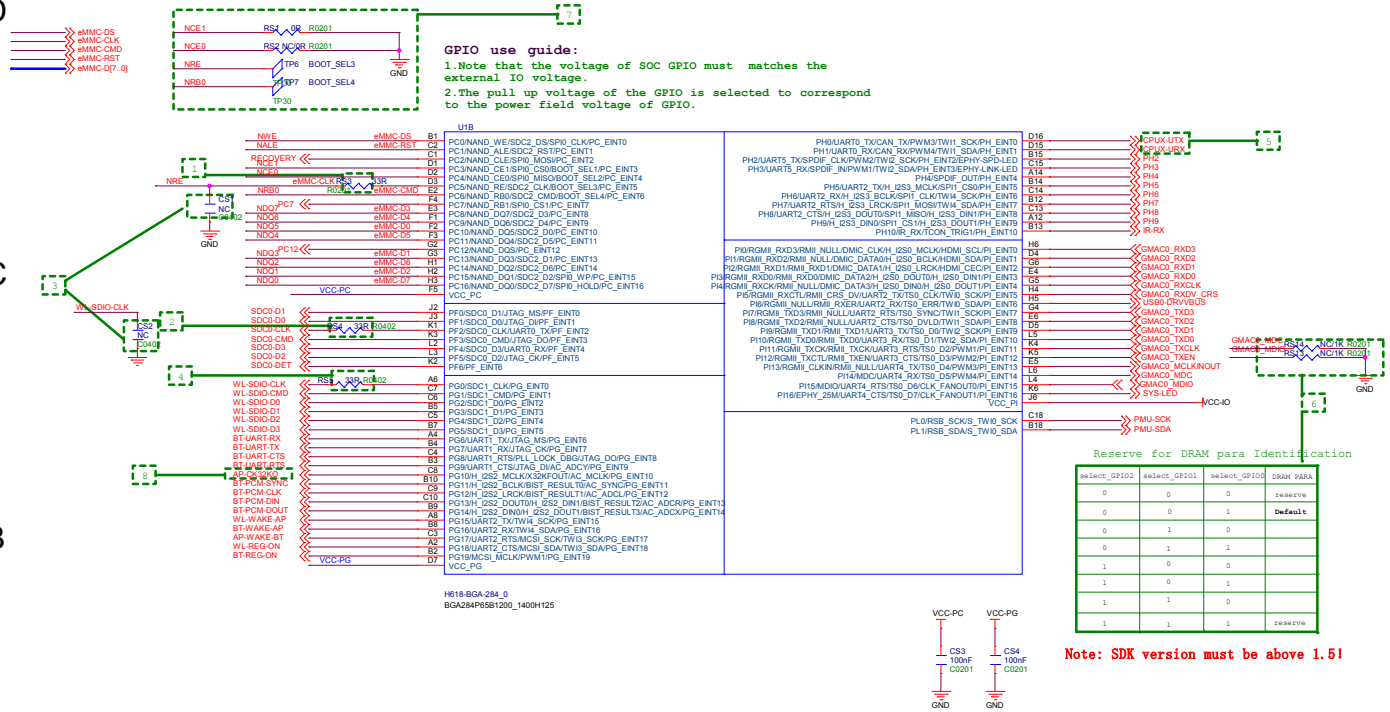
GPIO



Reserve for DRAM para Identification

select_GPIO2	select_GPIO1	select_GPIO0	DRAM PARA
0	0	0	reserve
0	0	1	**Default**
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	reserve

Note: SDK version must be above 1.51

SOC and peripheral circuit considerations-1

1.RS3 is the termination resistor at the source end of EMMC-CLK, which cannot be deleted.

2.RS4 is the termination resistor of SDC0-CLK source end, which cannot be deleted.

3.CS1 and CS2 are reserved for EMI suppression and need to be placed close to the Device.

4.RS5 is the termination resistor of SDIO-CLK source end, which cannot be deleted.

5.The default function of PH0 and PH1 is the UART print port, which is used for system software debugging and cannot be changed.

6.The DRAM para version identification reserved circuit cannot be deleted. For the purpose of software normalization management, the same firmware is compatible with multiple DRAM templates and DRAM materials. The way to read the hardware GPIO level in the boot phase, the software automatically calls the corresponding DRAM para. Pay special attention to the one-to-one correspondence between BOM and DRAM para.

7.boot sel: BROM will read the state of BOOT_Select, choose the external storage medium to boot, and speed up the boot time.
H616 has 4 boot sel pins multiplexed with the PC port, the configuration relationship is as follows:

bit[10]	bit[11]	bit[12]	bit[13]	Media
1	1	1	1	MLC/SLC NAND
0	1	1	1	eMMC USER ← Default
1	0	1	1	eMMC BOOT
1	1	0	1	SPI NOR
1	1	1	0	SPI NAND

The multiplexing relationship between 4 boot sel and PC port is as follows:
Bit[10]->PC3
Bit[11]->PC4
Bit[12]->PC5
Bit[13]->PC6

8.32K clock fanout, output low frequency clock, can be used by external wifi module, needs to surrounded by GND.

GPIO power domain list:

GROUP	Power Field	Voltage(V)
PC	VCC-PC	1.8/3.3
PF	VCC-PLL/VCC-IO	1.8/3.3
PG	VCC-PG	1.8/3.3
PH	VCC-IO	3.3
PI	VCC-PI	1.8/3.3
PL	VCC-PLL	1.8

Note: 1. When GPIO is not used, it can be directly floated, and the software is set to Disable.
2. After changing the default voltage of the multi-voltage IO power supply, the corresponding configuration changes must be confirmed on the software.

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SOC and peripheral circuit considerations-2

1. The HDMI differential signal controls the differential impedance of 100ohm.

2. REXT is a sensitive signal, and the layout path is kept to the shortest.

3. Lineout, TVOUT individually ground; TVOUT trace control impedance 37.5ohm.

4. USB differential signal control differential impedance 90ohm.

5. The decoupling capacitance of each module has been optimized by PI and cannot be modified.

6. The bypass capacitor of CODEC cannot be modified. These parameters will affect the internal power-on sequence.

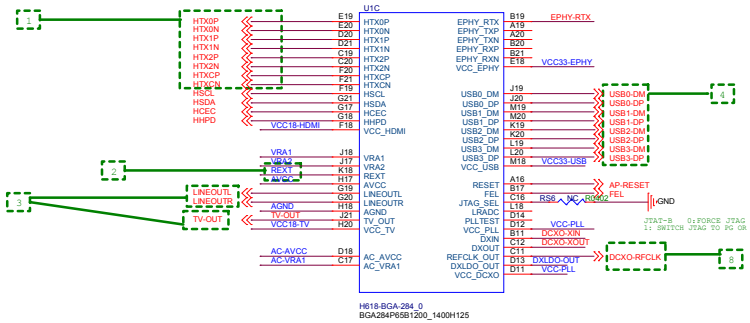
7. The AGND trace should be as wide as possible, at least 12mil or more, and the copper skin should be widened after the BGA is released; the number of R99 GND vias should be guaranteed at least two.

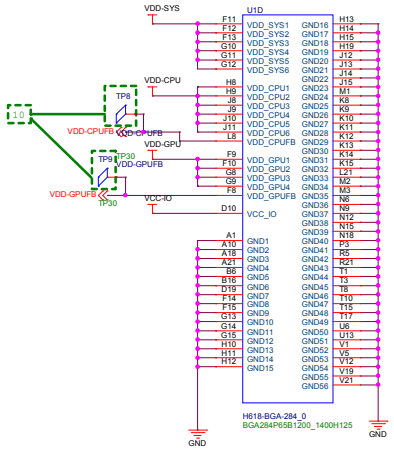
8. 24Mfanout clock, can be used for wifi module, and the wiring needs to be isolated with ground.

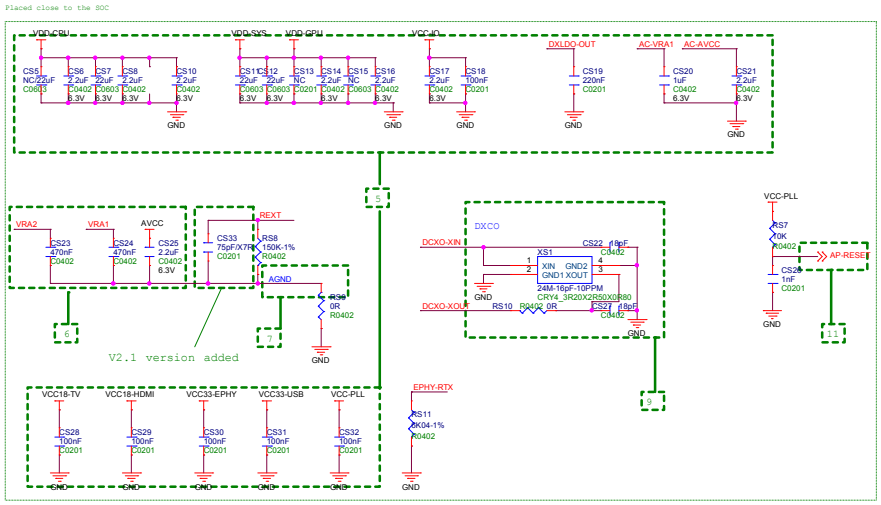
9. The crystal matching capacitor is the reference value, the actual capacitance value can be modified according to the test; in addition, the series resistance needs to be reserved to facilitate debugging the oscillation amplitude.

10. The voltage feedback test point should be placed near the projection area of the back of the power pin.

11. The system reset signal AP-reset is far away from the board edge and interference signals.







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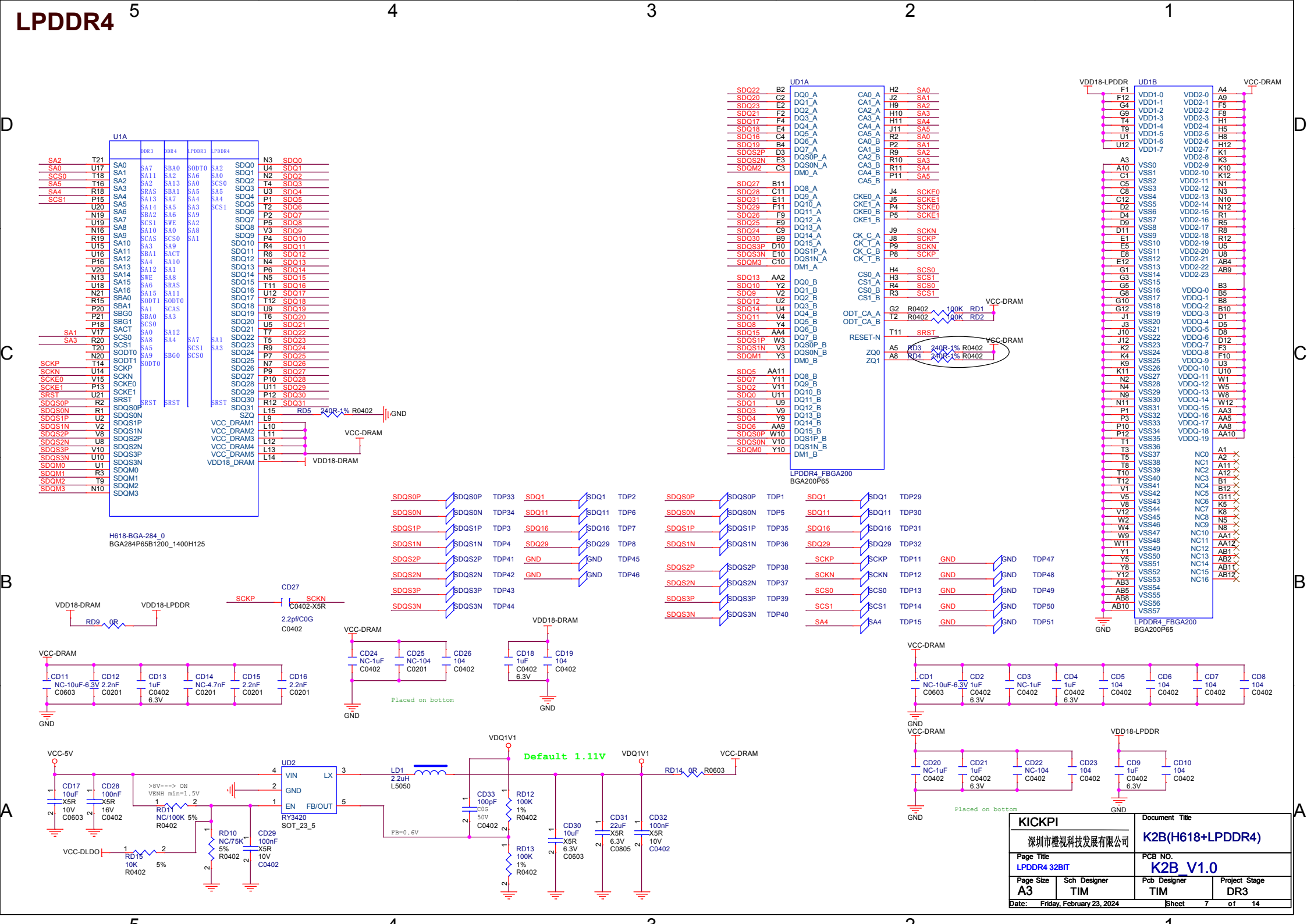
LPDDR4


U1A
H618-BGA-284_0
BGA284P65B1200_1400H125
UD1A
LPDDR4_FBGA200
BGA200P65
UD1B
LPDDR4_FBGA200
BGA200P65
VCC-DRAM
VDD18-DRAM
VDD18-LPDDR
VCC-5V
VCC-DLDO
GND
VDQ1V1
Default 1.11V
UD2
RY3420
SOT_23_5
LD1
2.2uH
L5050
Placed on bottom
KICKPI
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LPDDR4 32BIT
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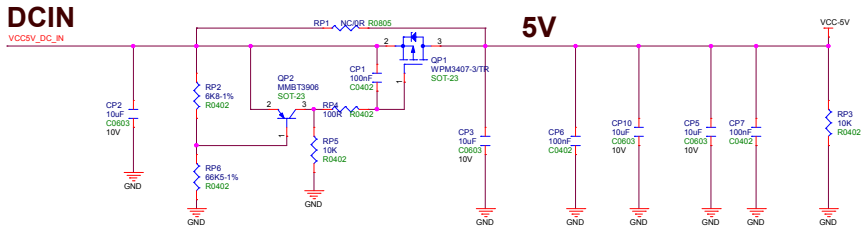
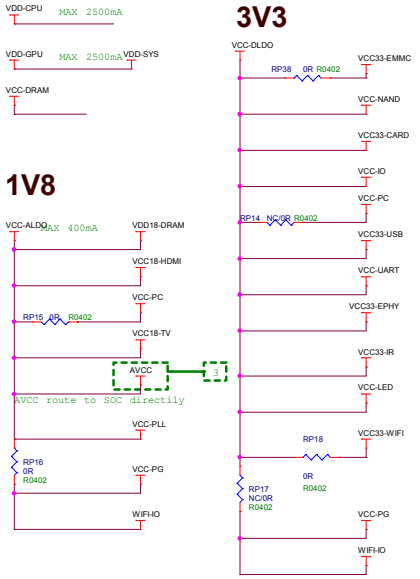
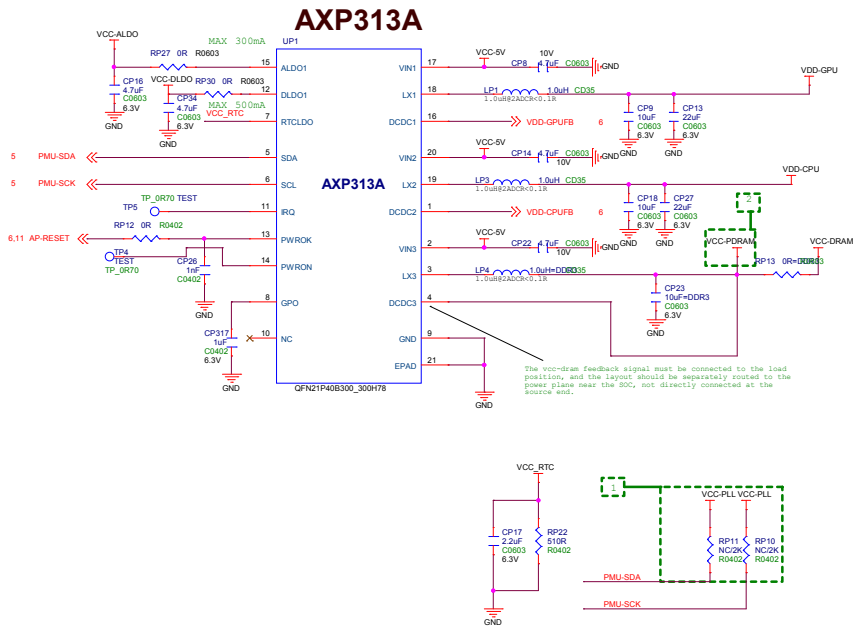
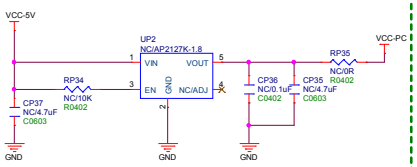






Option1:



Reserve for EMMC which 1.8V current greater than 300mA.

Power design considerations

1. AXP313A is controlled by the I2C signal of the PL port, and the external needs to be reserved for pull-up to VCC-PLL.

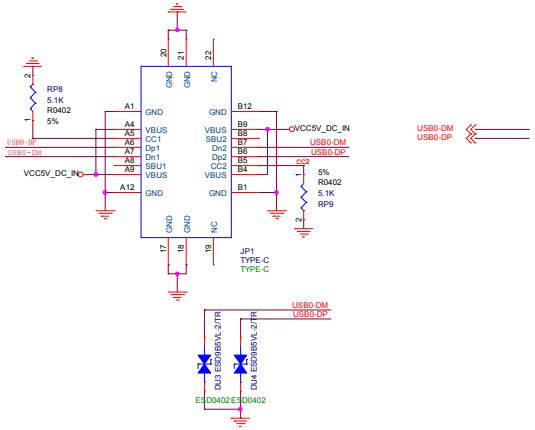
2. VCC-DRAM can support DDR3, DDR4, LPDDR3, LPDDR4 different DRAM power supply, different DRAM types through software
The identification is automatically matched to the appropriate supply voltage.

3. AVCC supplies power for analog modules such as Audio codec, T-senor, etc. The accuracy must be +/- 1%, and the minimum power supply voltage cannot be lower than 1.78V.
Otherwise, it will affect Audio performance and sensor accuracy.

Important:

The stability of the power supply directly affects the stability of the system. Please be sure to refer to the relevant guide in the "Hardware Design Guide" for the schematic diagram and PCB design!

Type-C OTG (USB2.0)



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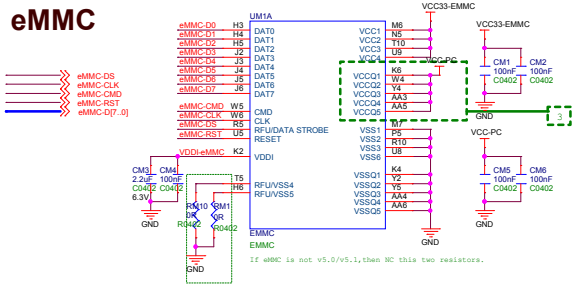
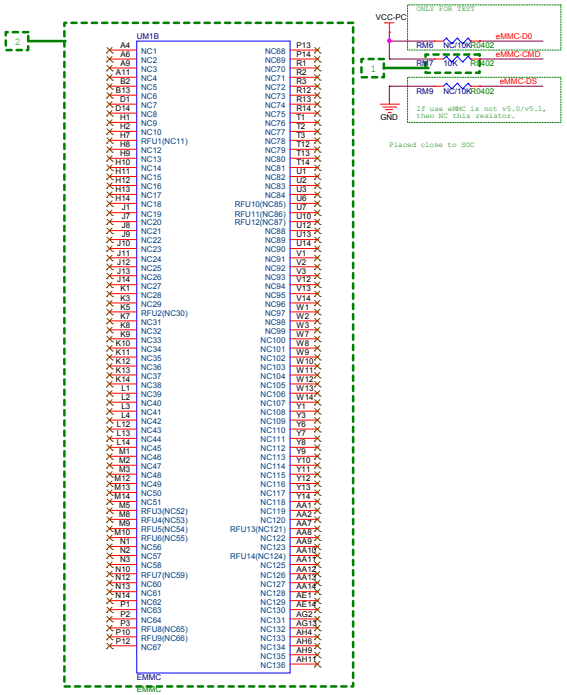
eMMC





Flash design considerations

1. CMD needs to be pulled up to VCC-PC.

2. The reserved pins, such as eMMCNC / RFU, are left unconnected. Do not connect these signals with power, ground, or other eMMC signals for easy fanout.

3. The EMMC IO power supply voltage matches the power domain voltage of the SOC GPIO.

Important:

For the PCB design of the Flash module, please refer to the layout guide in the Hardware Design Guide,
The guide has detailed impedance, timing and crosstalk requirements;
Note that when EMMC and NAND are dual-layout, a daisy-chain topology is used, and EMMC is used as a routing terminal.

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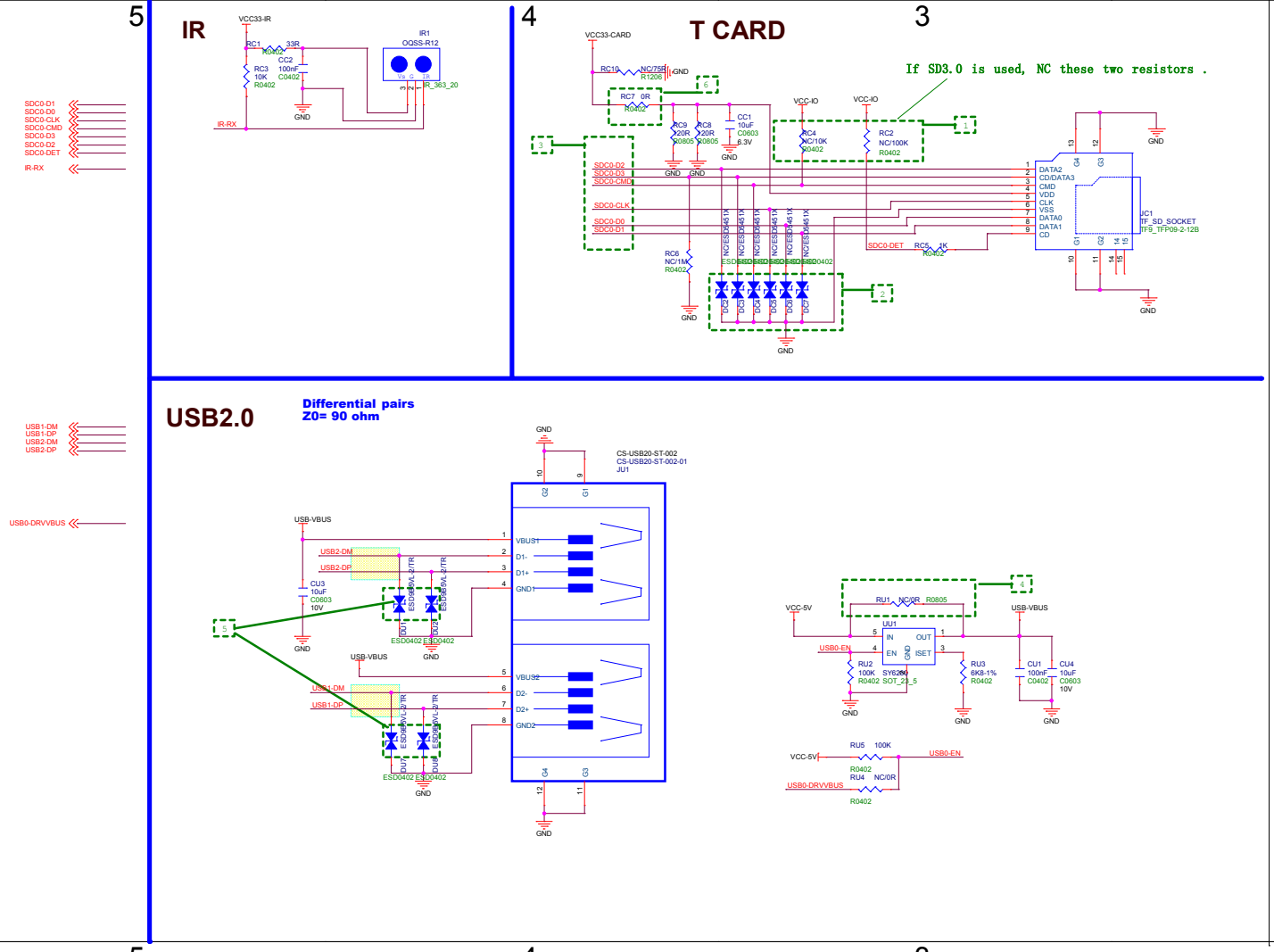

Peripheral interface considerations-1

1. card IO supports internal 1.8V / 3.3V automatic switching, the default is 3.3V, SDC0_CMD and SDC0_DET signals have weak pull-ups internally,
External pull-ups need to be reserved to prevent insufficient internal pull-ups.

2. The parasitic capacitance of the ESD device cannot be greater than 10pF, otherwise it will affect the signal quality.

3. Please refer to the relevant guide of "Hardware Design Guide" for the design of SDIO signal layout. The guide has detailed impedance, timing and crosstalk requirements.

4. Reserve 0R resistor for easy debugging.

5. USB2.0 interface signal lines USB0-DM, USB0-DP, USB1-DM, USB1-DP, USB3-DM, USB3-DP are high-speed signal lines, and connected ESD devices
Low capacitance value is required, otherwise it will affect data transmission, it is better to be less than or equal to 4pF. The USB differential signal controls the differential impedance of 90ohm and is isolated around the ground.

6. Connect a 0 ohm resistor in series to prevent the card from causing the power to drop instantly.

Important:

For ESD device layout related specifications, please refer to the relevant guides in the "Hardware Design Guide" for detailed instructions.

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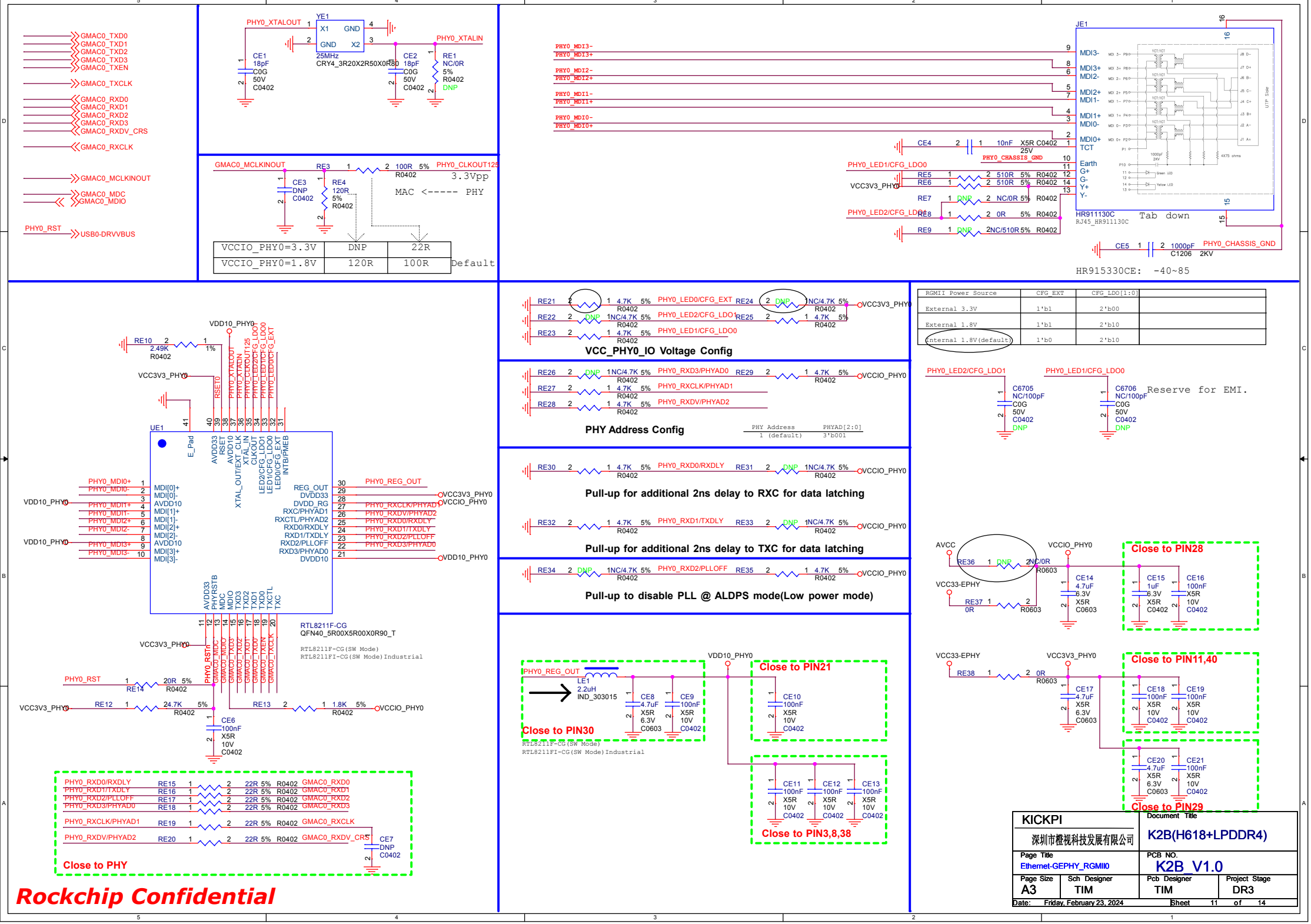
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
PHY0_RST
USB0-DRVVBUS
PHY0_XTALOUT
YE1
X1
GND
X2
25MHz
CRY4_3R20X2R50X0R80
PHY0_XTALIN
CE1
18pF
C0G
50V
C0402
CE2
18pF
C0G
50V
C0402
RE1
NC/0R
5%
R0402
DNP
GMAC0_MCLKINOUT
RE3
100R 5%
R0402
PHY0_CLKOUT125
3.3Vpp
CE3
DNP
C0402
RE4
120R
5%
R0402
MAC <----- PHY
VCCIO_PHY0=3.3V | DNP | 22R
VCCIO_PHY0=1.8V | 120R | 100R | Default
PHY0_MDI3-
PHY0_MDI3+
PHY0_MDI2-
PHY0_MDI2+
PHY0_MDI1-
PHY0_MDI1+
PHY0_MDI0-
PHY0_MDI0+
JE1
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
TCT
Earth
G+
G-
Y+
Y-
CE4
10nF X5R C0402
25V
PHY0_CHASSIS_GND
PHY0_LED1/CFG_LDO0
RE5
510R 5% R0402
RE6
510R 5% R0402
VCC3V3_PHY0
RE7
DNP
NC/0R 5% R0402
PHY0_LED2/CFG_LDO1
RE8
0R 5% R0402
RE9
DNP
NC/510R 5% R0402
HR911130C
RJ45_HR911130C
Tab down
CE5
1000pF
C1206 2KV
PHY0_CHASSIS_GND
HR915330CE: -40~85
VDD10_PHY0
RE10
2.49K
1%
R0402
VCC3V3_PHY0
RSET0
PHY0_XTALOUT
PHY0_XTALIN
PHY0_CLKOUT125
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
PHY0_LED0/CFG_EXT
UE1
E_Pad
AVDD33
RSET
AVDD11
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
VCC3V3_PHY0
VCCIO_PHY0
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
VDD10_PHY0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
PHY0_RSTn
GMAC0_MDC
GMAC0_MDIO
GMAC0_TXD3
GMAC0_TXD2
GMAC0_TXD1
GMAC0_TXD0
GMAC0_TXCTL
GMAC0_TXCLK
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
PHY0_RST
RE14
20R 5%
R0402
VCC3V3_PHY0
RE12
24.7K 5%
R0402
RE13
1.8K 5%
R0402
VCCIO_PHY0
CE6
100nF
X5R
10V
C0402
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
RE15
RE16
RE17
RE18
22R 5% R0402
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
PHY0_RXCLK/PHYAD1
RE19
GMAC0_RXCLK
PHY0_RXDV/PHYAD2
RE20
GMAC0_RXDV_CRS
CE7
DNP
C0402
Close to PHY
RE21
4.7K 5%
R0402
PHY0_LED0/CFG_EXT
RE22
DNP
NC/4.7K 5%
PHY0_LED2/CFG_LDO1
RE23
PHY0_LED1/CFG_LDO0
RE24
DNP
NC/4.7K 5%
RE25
4.7K 5%
VCC3V3_PHY0
VCC_PHY0_IO Voltage Config
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V(default) | 1'b0 | 2'b10
RE26
PHY0_RXD3/PHYAD0
RE27
PHY0_RXCLK/PHYAD1
RE28
PHY0_RXDV/PHYAD2
RE29
VCCIO_PHY0
PHY Address | PHYAD[2:0]
1 (default) | 3'b001
PHY Address Config
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
C6705
NC/100pF
C6706
NC/100pF
Reserve for EMI.
RE30
PHY0_RXD0/RXDLY
RE31
Pull-up for additional 2ns delay to RXC for data latching
RE32
PHY0_RXD1/TXDLY
RE33
Pull-up for additional 2ns delay to TXC for data latching
RE34
PHY0_RXD2/PLLOFF
RE35
Pull-up to disable PLL @ ALDPS mode(Low power mode)
AVCC
RE36
DNP
NC/0R
R0603
VCCIO_PHY0
VCC33-EPHY
RE37
0R
R0603
CE14
4.7uF
6.3V
X5R
C0603
Close to PIN28
CE15
1uF
6.3V
X5R
C0402
CE16
100nF
X5R
10V
C0402
VCC33-EPHY
RE38
0R
R0603
VCC3V3_PHY0
CE17
4.7uF
6.3V
X5R
C0603
Close to PIN11,40
CE18
100nF
X5R
10V
C0402
CE19
100nF
X5R
10V
C0402
CE20
4.7uF
X5R
6.3V
C0603
CE21
100nF
X5R
10V
C0402
Close to PIN29
PHY0_REG_OUT
LE1
2.2uH
IND_303015
CE8
4.7uF
X5R
6.3V
C0603
CE9
100nF
X5R
10V
C0402
Close to PIN30
VDD10_PHY0
CE10
100nF
X5R
10V
C0402
Close to PIN21
CE11
100nF
X5R
10V
C0402
CE12
100nF
X5R
10V
C0402
CE13
100nF
X5R
10V
C0402
Close to PIN3,8,38
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KICKPI
深圳市橙视科技发展有限公司
Document Title
K2B(H618+LPDDR4)
Page Title
Ethernet-GEPHY_RGMII0
PCB NO.
K2B_V1.0
Page Size
A3
Sch Designer
TIM
Pcb Designer
TIM
Project Stage
DR3
Date: Friday, February 23, 2024
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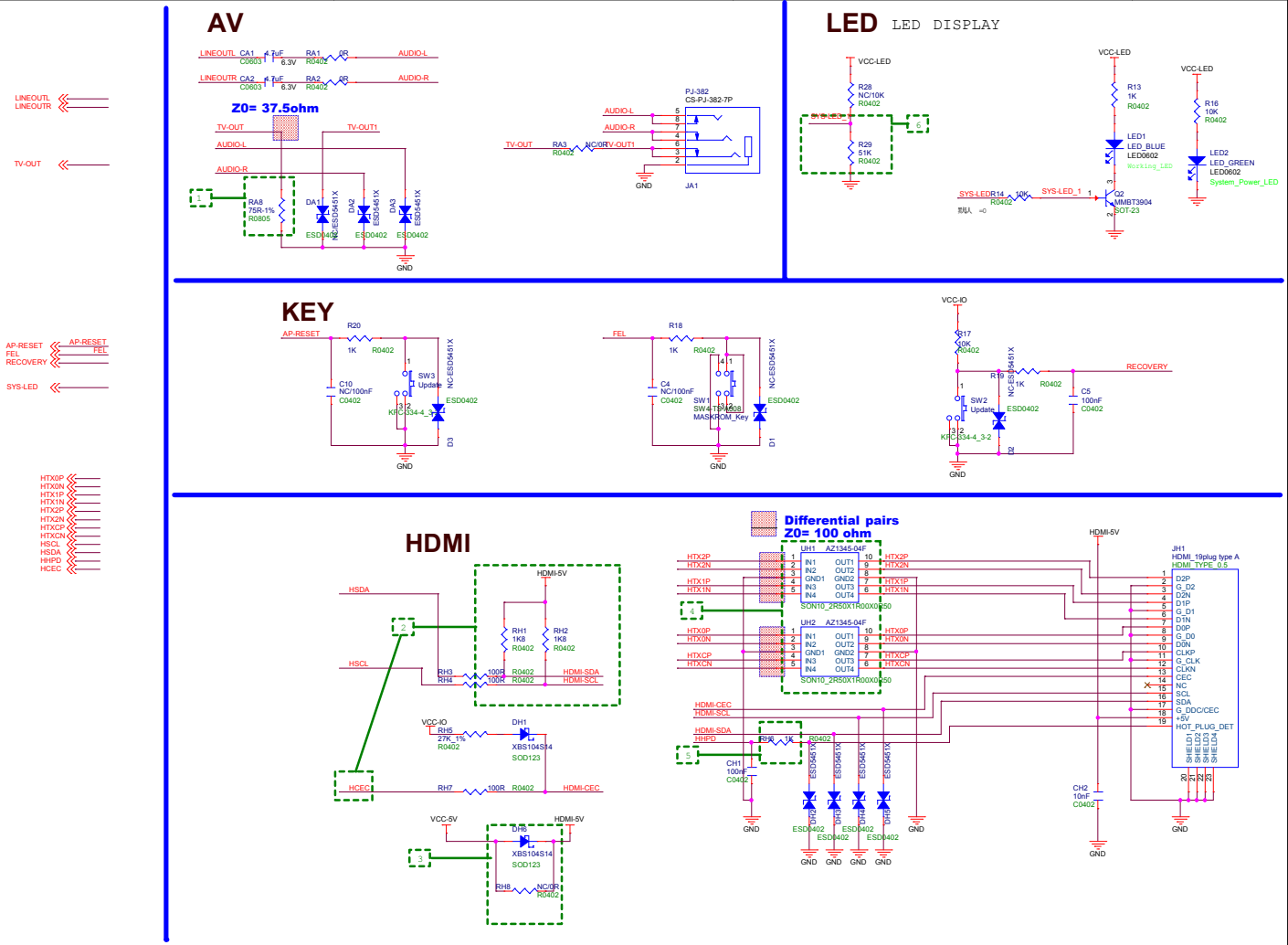

Audio&HDMI Interface considerations

1. The 75 ohm resistor of the CVBS port needs to use the 0805 package, because the CVBS output current type, the current will flow through the resistor, if the resistor package is too small ,The resistor will be burned by heat.

2.H616 HDMI IIC and CEC have built-in levelshift circuit, which supports direct connection to device.

3. The 5V power supply of HDMI must be connected in series with Schottky diodes to prevent leakage of the TV after shutdown. The voltage drop of ordinary diodes is high, which is easy to cause HDMI power supply is lower than 4.75v, to avoid compatibility problems, please choose a Schottky diode with reduced on-voltage.

4. The dynamic resistance (Rdyn) of the ESD device used on the HDMI differential line is less than 0.35 ohms, the operating voltage is 5v, and the parasitic capacitance is less than 0.35pF,It is recommended to use AZ1345-04F.

5.HPD has a built-in levelshift circuit in H616, which can withstand 5V, so it can be directly connected in series with no voltage division.

6. The SYS-LED power-on default is low, add a pull-down resistor to stabilize the level.

Important:

For audio and HDMI differential layout, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.

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Page Title: AV-HDMI-KEY-LED	PCB NO.: K2B_V1.0
Page Size: Custom / Sch Designer: TIM	Pcb Designer: TIM / Project Stage: DR3
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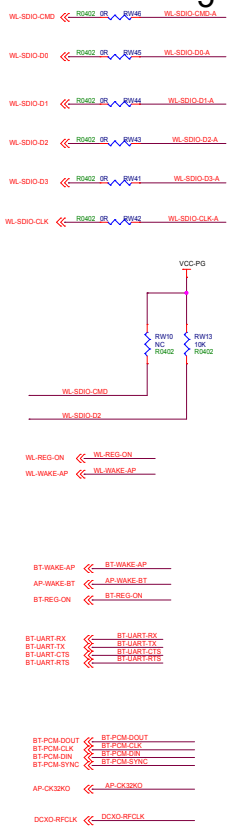
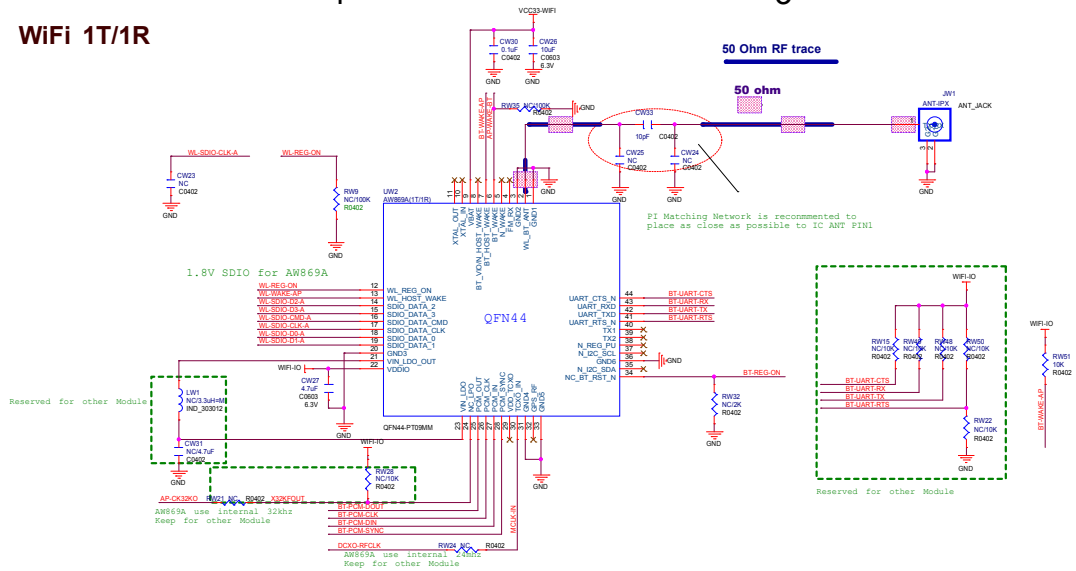
WiFi 1T/1R





WIFI module design considerations

Important:

For SDIO and RF antenna layout, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.

KICKPI 深圳市橙视科技发展有限公司	Document Title: K2B(H618+LPDDR4)
Page Title: WIFI-BT 1T/1R	PCB NO.: K2B_V1.0
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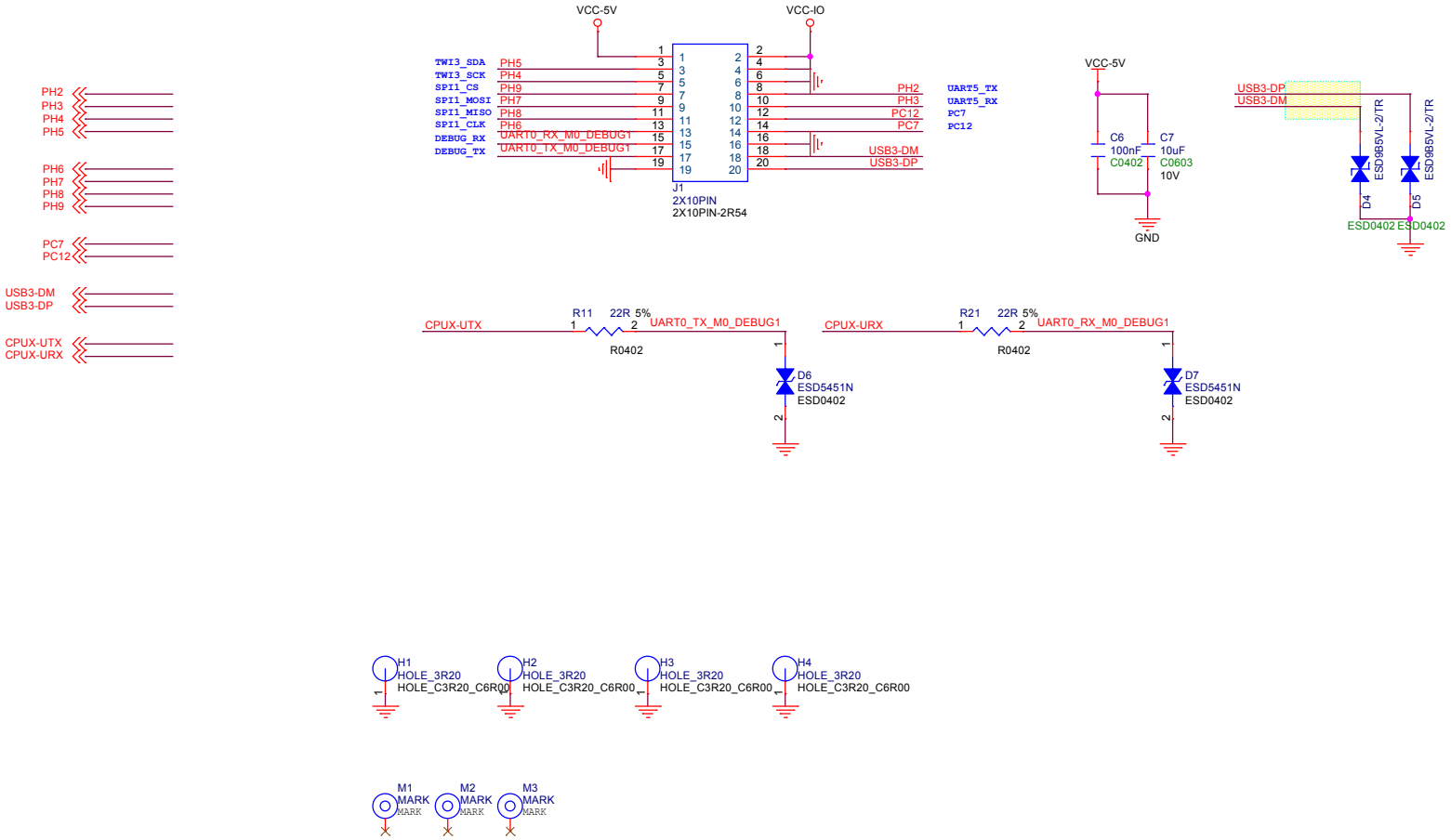

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Page Title GPIO/Debug UART		PCB NO. K2B_V1.0	
Page Size A3	Sch Designer TIM	Pcb Designer TIM	Project Stage DR3
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