# REVISION HISTORY

| Revision | Description | Date | Drawn | Checked |
|---|---|---|---|---|
| Ver 1.0 | Initial Version | 2022-04-27 | HHY | |

## Schematics Index:





AllWinner Technology Co.,Ltd

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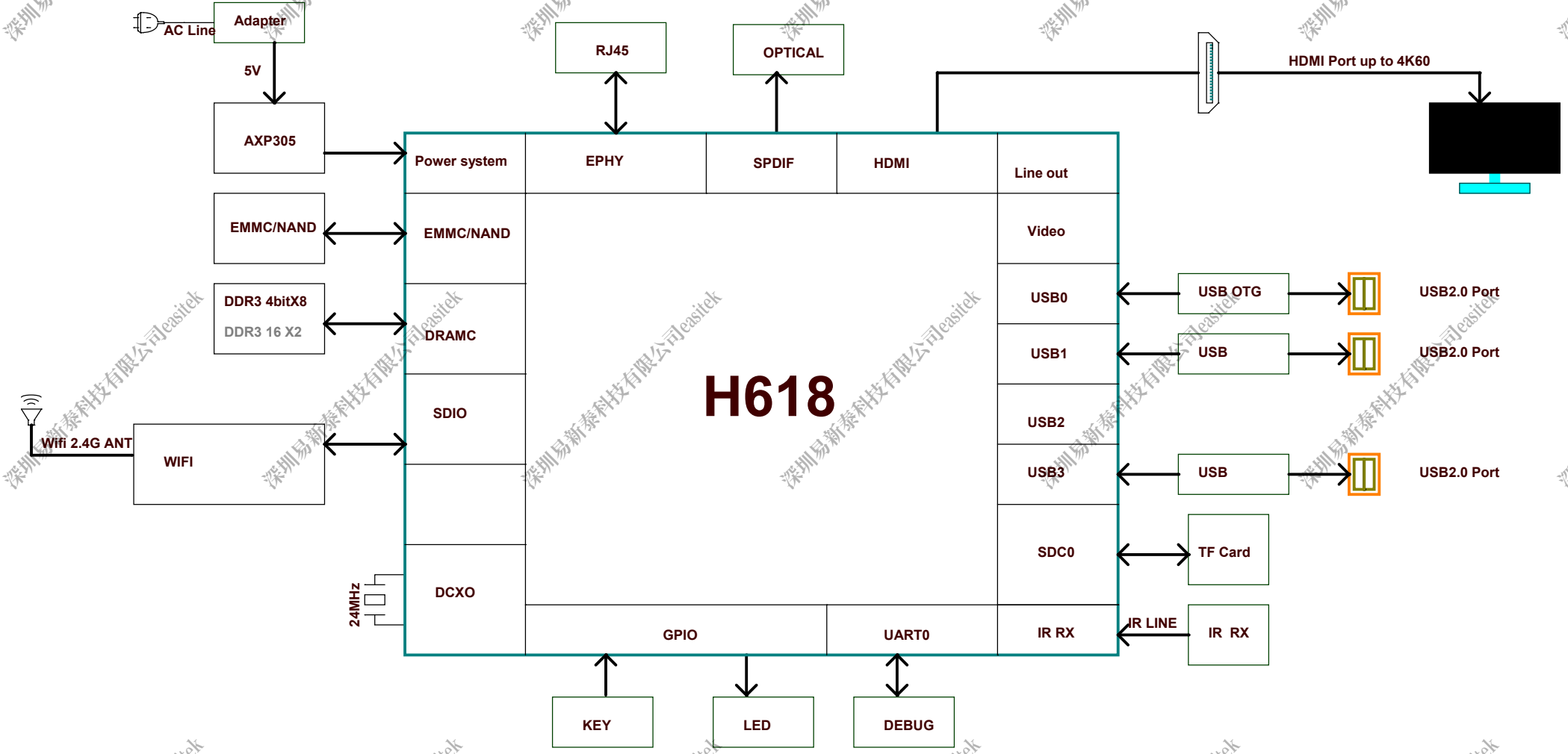
# BLOCK



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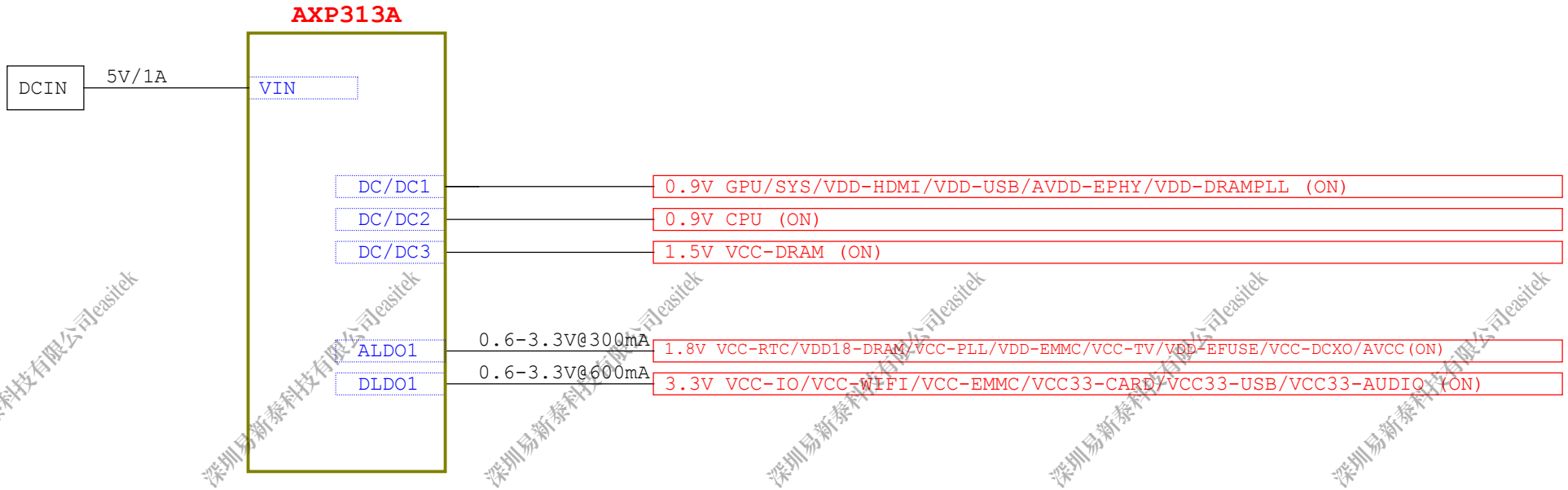
# POWER TREE

DEFAULT POWER ON

DEFAULT POWER OFF



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# GPIO ASSIGNMENT

| PIN | Define | CFG | Function |
|---|---|---|---|
| PC0 | NAND_WE/SDC2_DS | 2/3 | NAND/eMMC |
| PC1 | NAND_ALE/SDC2_RST | 2/3 | |
| PC2 | NAND_CLE | 2 | |
| PC3 | NAND_CE1 | 2 | |
| PC4 | NAND_CE0 | 2 | |
| PC5 | NAND_RE/SDC2_CLK | 2/3 | |
| PC6 | NAND_RB0/SDC2_CMD | 2/3 | |
| PC7 | NAND_RB1 | 2 | |
| PC8 | NAND_DQ7/SDC2_D3 | 2/3 | |
| PC9 | NAND_DQ6/SDC2_D4 | 2/3 | |
| PC10 | NAND_DQ5/SDC2_D0 | 2/3 | |
| PC11 | NAND_DQ4/SDC2_D5 | 2/3 | |
| PC12 | NAND_DQS | 2 | |
| PC13 | NAND_DQ3/SDC2_D1 | 2/3 | |
| PC14 | NAND_DQ2/SDC2_D6 | 2/3 | |
| PC15 | NAND_DQ1/SDC2_D2 | 2/3 | |
| PC16 | NAND_DQ0/SDC2_D7 | 2/3 | |

| PIN | Define | CFG | Function |
|---|---|---|---|
| PF0 | SDC0_D1 | 2 | CARD0 |
| PF1 | SDC0_D0 | 2 | |
| PF2 | SDC0_CLK/UART0_TX | 2/3 | |
| PF3 | SDC0_CMD | 2 | |
| PF4 | SDC0_D3/UART0_RX | 2/3 | |
| PF5 | SDC0_D2 | 2 | |
| PF6 | SDC0-DET | 2 | |

| PIN | Define | CFG | Function |
|---|---|---|---|
| PG0 | SDC1_CLK | 2 | WIFI+BT |
| PG1 | SDC1_CMD | 2 | |
| PG2 | SDC1_D0 | 2 | |
| PG3 | SDC1_D1 | 2 | |
| PG4 | SDC1_D2 | 2 | |
| PG5 | SDC1_D3 | 2 | |
| PG6 | UART1_TX | 2 | |
| PG7 | UART1_RX | 2 | |
| PG8 | UART1_RTS | 2 | |
| PG9 | UART1_CTS | 2 | |
| PG10 | AP-CK32KO | 3 | |
| PG11 | PCM2_SYNC | 2 | |
| PG12 | PCM2_CLK | 2 | |
| PG13 | PCM2_DOUT | 2 | |
| PG14 | PCM2_DIN | 2 | |
| PG15 | WL-WAKE-AP | 0 | |
| PG16 | BT-WAKE-AP | 0 | |
| PG17 | AP-WAKE-BT | 1 | |
| PG18 | WL-REG-ON | 1 | |
| PG19 | BT-REG-ON | 1 | |

| PIN | Define | CFG | Function |
|---|---|---|---|
| PH0 | CPUX-UTX | 2 | |
| PH1 | CPUX-URX | 2 | |
| PH2 | FD628-SCK | X | |
| PH3 | FD628-SDA | X | |
| PH4 | SPDIF-OUT | 3 | |
| PH5 | | 1 | |
| PH6 | SYS-LED | 1 | |
| PH7 | | 1 | |
| PH8 | USB0-DRVVBUS | 1 | |
| PH9 | RECOVERY | 0 | |
| PH10 | IR-RX | 3 | |

X: Network port lights need to be configured

| PIN | Define | CFG | Function |
|---|---|---|---|
| PI0 | | | |
| PI1 | | | |
| PI2 | | | |
| PI3 | | | |
| PI4 | | | |
| PI5 | | | |
| PI6 | | | |
| PI7 | | | |
| PI8 | | | |
| PI9 | | | |
| PI10 | | | |
| PI11 | | | |
| PI12 | | | |
| PI13 | | | |
| PI14 | | | |
| PI15 | | | |
| PI16 | | | |

| PIN | Define | CFG | Function |
|---|---|---|---|
| PL0 | PMU-SCK | 2 | |
| PL1 | PMU-SDA | 2 | |



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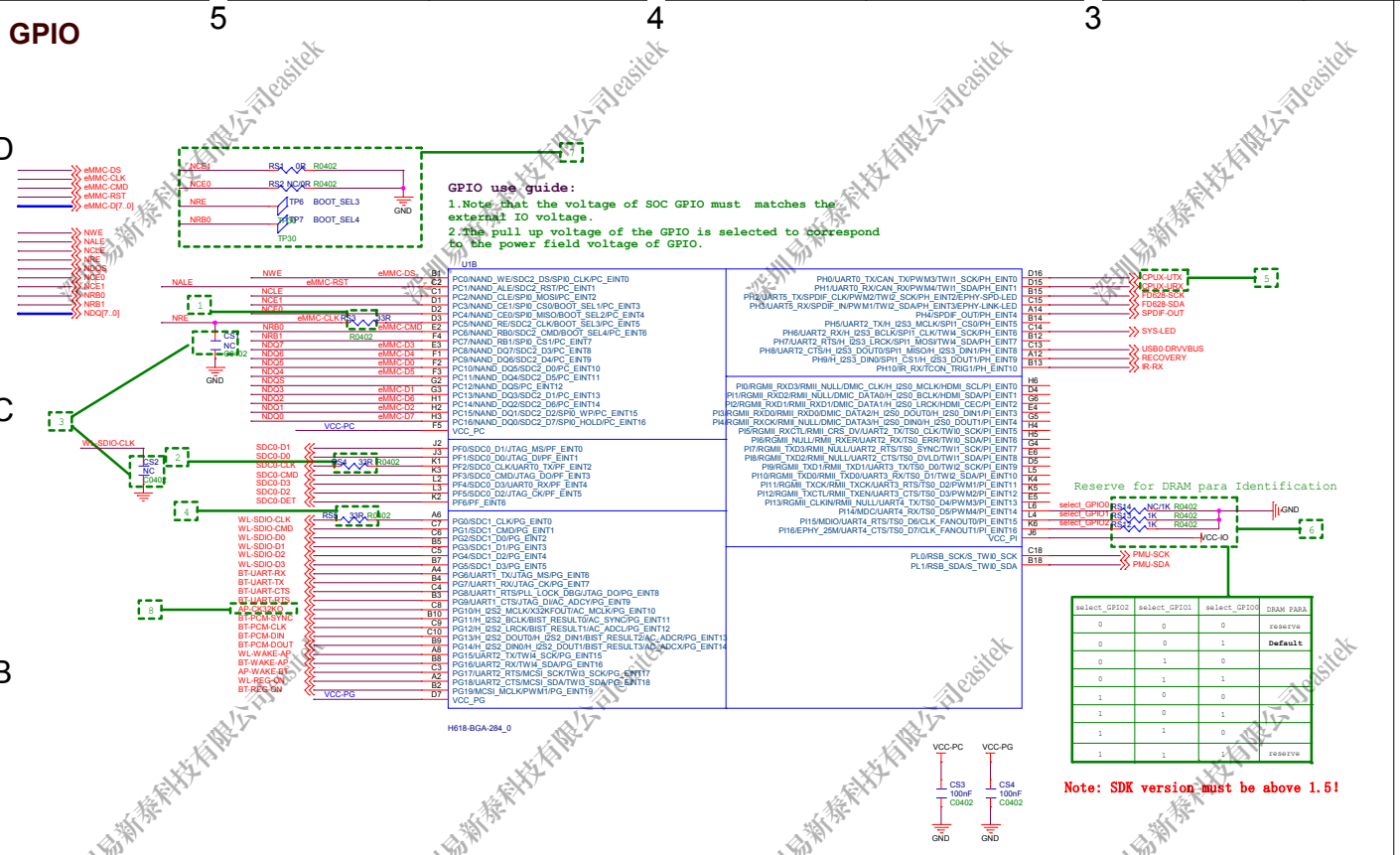


# SOC and peripheral circuit considerations-1

1. RS3 is the termination resistor at the source end of EMMC-CLK, which cannot be deleted.

2. RS4 is the termination resistor of SDCO-CLK source end, which cannot be deleted.

3. CS1 and CS2 are reserved for EMI suppression and need to be placed close to the Device.

4. RS5 is the termination resistor of SDIO-CLK source end, which cannot be deleted.

5. The default function of PH0 and PH1 is the UART print port, which is used for system software debugging and cannot be changed.

6. The DRAM para version identification reserved circuit cannot be deleted. For the purpose of software normalization management, the same firmware is compatible with multiple DRAM templates and DRAM materials. The way to read the hardware GPIO level is in the boot phase, the software automatically calls the corresponding DRAM para. Pay special attention to the one-to-one correspondence between BOM and DRAM para.

7. boot sel: BROM will read the state of BOOT_Select, choose the external storage medium to boot, and speed up the boot time.
H616 has 4 boot sel pins multiplexed with the PC port, the configuration relationship is as follows:

| bit[10] | bit[11] | bit[12] | bit[13] | Media | |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | MLC/SLC NAND | |
| 0 | 1 | 1 | 1 | eMMC USER | Default |
| 1 | 0 | 1 | 1 | eMMC BOOT | |
| 1 | 1 | 0 | 1 | SPI NOR | |
| 1 | 1 | 1 | 0 | SPI NAND | |

The multiplexing relationship between 4 boot sel and PC port is as follows:
Bit[10]->PC3
Bit[11]->PC4
Bit[12]->PC5
Bit[13]->PC6

8. 32K clock fanout, output low frequency clock, can be used by external wifi module, needs to surrounded by GND.

GPIO power domain list:

| GROUP | Power Field | Voltage(V) |
|---|---|---|
| PC | VCC-PC | 1.8/3.3 |
| PF | VCC-PLL/VCC-IO | 1.8/3.3 |
| PG | VCC-PG | 1.8/3.3 |
| PH | VCC-IO | 3.3 |
| PI | VCC-PI | 1.8/3.3 |
| PL | VCC-PLL | 1.8 |

Note: 1. When GPIO is not used, it can be directly floated, and the software is set to Disable.
2. After changing the default voltage of the multi-voltage IO power supply, the corresponding configuration changes must be confirmed on the software.

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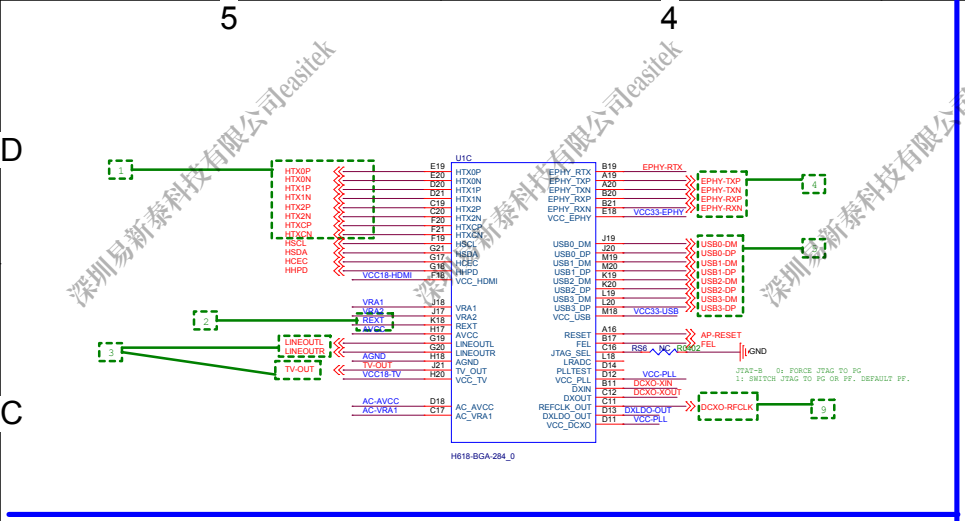
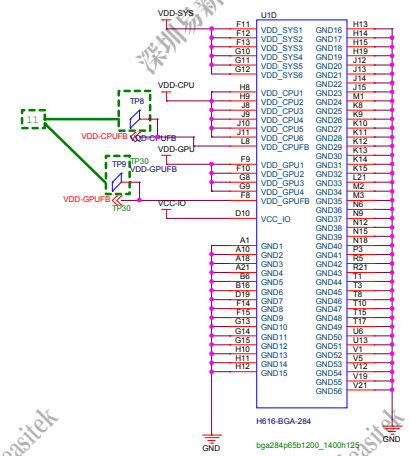
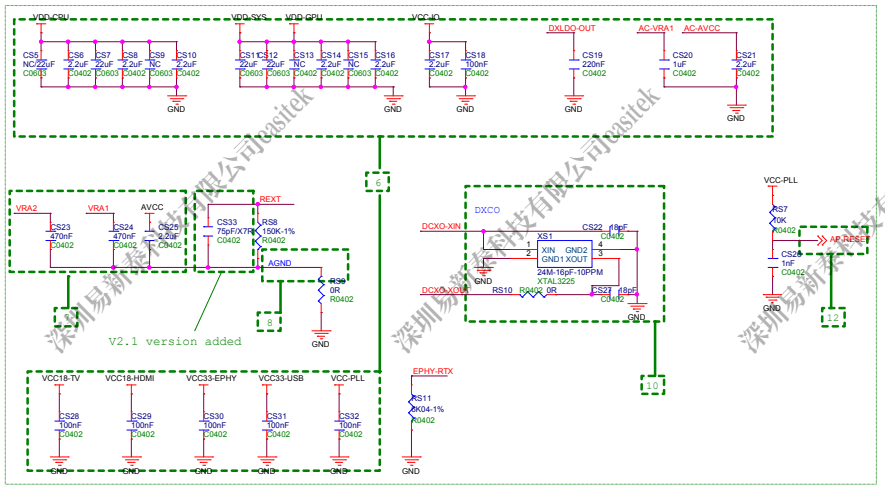



Placed close to the SOC




# SOC and peripheral circuit considerations-2

1. The HDMI differential signal controls the differential impedance of 100ohm.
2. REXT is a sensitive signal, and the layout path is kept to the shortest.
3. Lineout, TVOUT individually ground; TVOUT trace control impedance 37.5ohm.
4. ePHY differential signal control differential impedance 100ohm.
5. USB differential signal control differential impedance 90ohm.
6. The decoupling capacitance of each module has been optimized by PI and cannot be modified.
7. The bypass capacitor of CODEC cannot be modified. These parameters will affect the internal power-on sequence.
8. The AGND trace should be as wide as possible, at least 12mil or more, and the copper skin should be widened after the BGA is released; the number of R99 GND vias should be guaranteed at least two.
9. 24Mfanout clock, can be used for wifi module, and the wiring needs to be isolated with ground.
10. The crystal matching capacitor is the reference value, the actual capacitance value can be modified according to the test; in addition, the series resistance needs to be reserved to facilitate debugging the oscillation amplitude.
11. The voltage feedback test point should be placed near the projection area of the back of the power pin.
12. The system reset signal AP-reset is far away from the board edge and interference signals.

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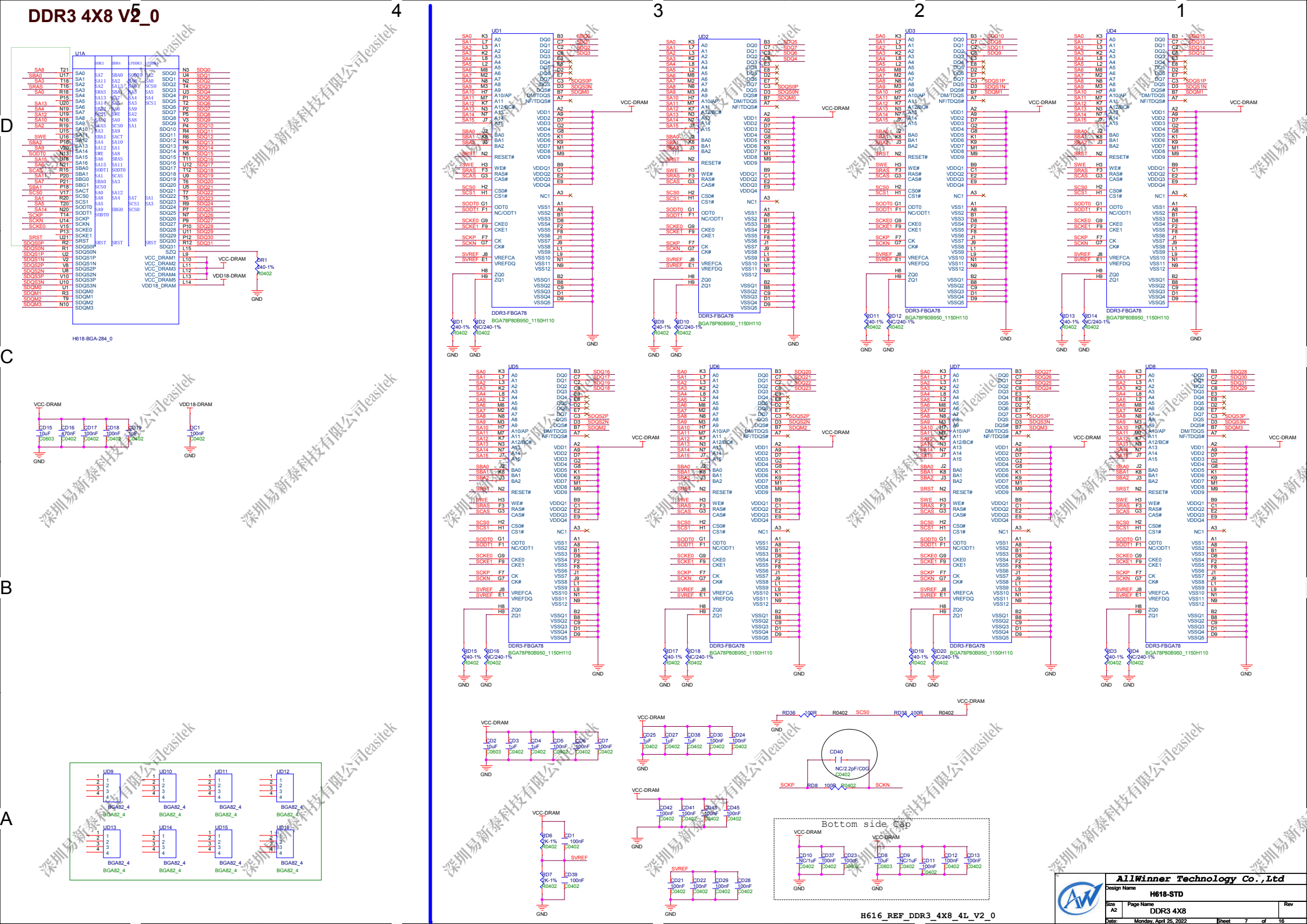
DDR3 4X8 V2_0
5
4
3
2
1
D
C
B
A
U1A
H618-BGA-284_0
UD1
UD2
UD3
UD4
UD5
UD6
UD7
UD8
DDR3-FBGA78
BGA78P80B950_1150H110
UD9
UD10
UD11
UD12
UD13
UD14
UD15
UD16
BGA82_4
VCC-DRAM
VDD18-DRAM
GND
Bottom side Cap
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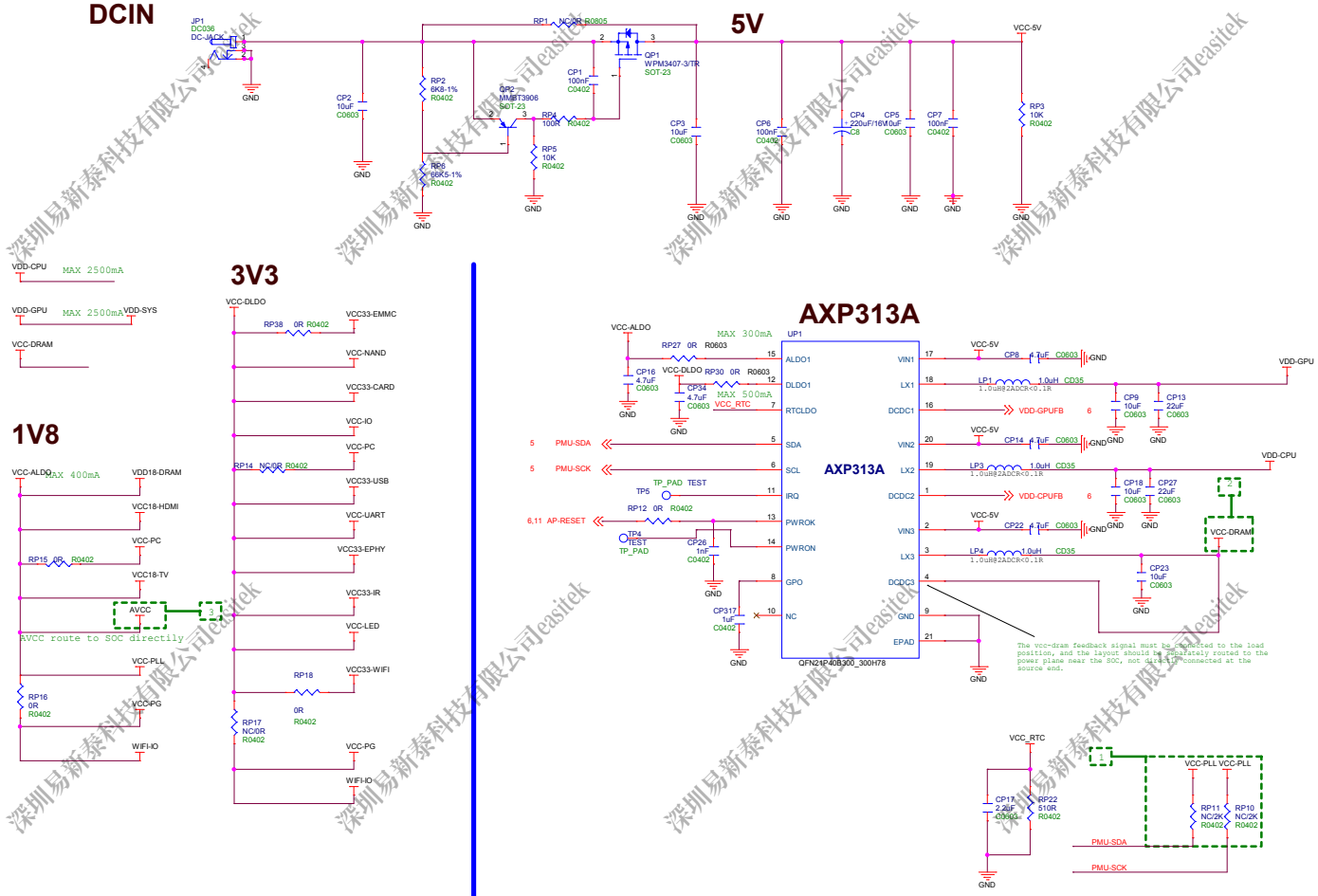


## Power design considerations

1. AXP313A is controlled by the I2C signal of the PL port, and the external needs to be reserved for pull-up to VCC-PLL.

2. VCC-DRAM can support DDR3, DDR4, LPDDR3, LPDDR4 different DRAM power supply, different DRAM types through software
The identification is automatically matched to the appropriate supply voltage.

3. AVCC supplies power for analog modules such as Audio codec, T-senor, etc. The accuracy must be +/-1%, and the minimum power supply voltage cannot be lower than 1.78V.
Otherwise, it will affect Audio performance and sensor accuracy.

**Important:**

*The stability of the power supply directly affects the stability of the system. Please be sure to refer to the relevant guide in the "Hardware Design Guide" for the schematic diagram and PCB design!*

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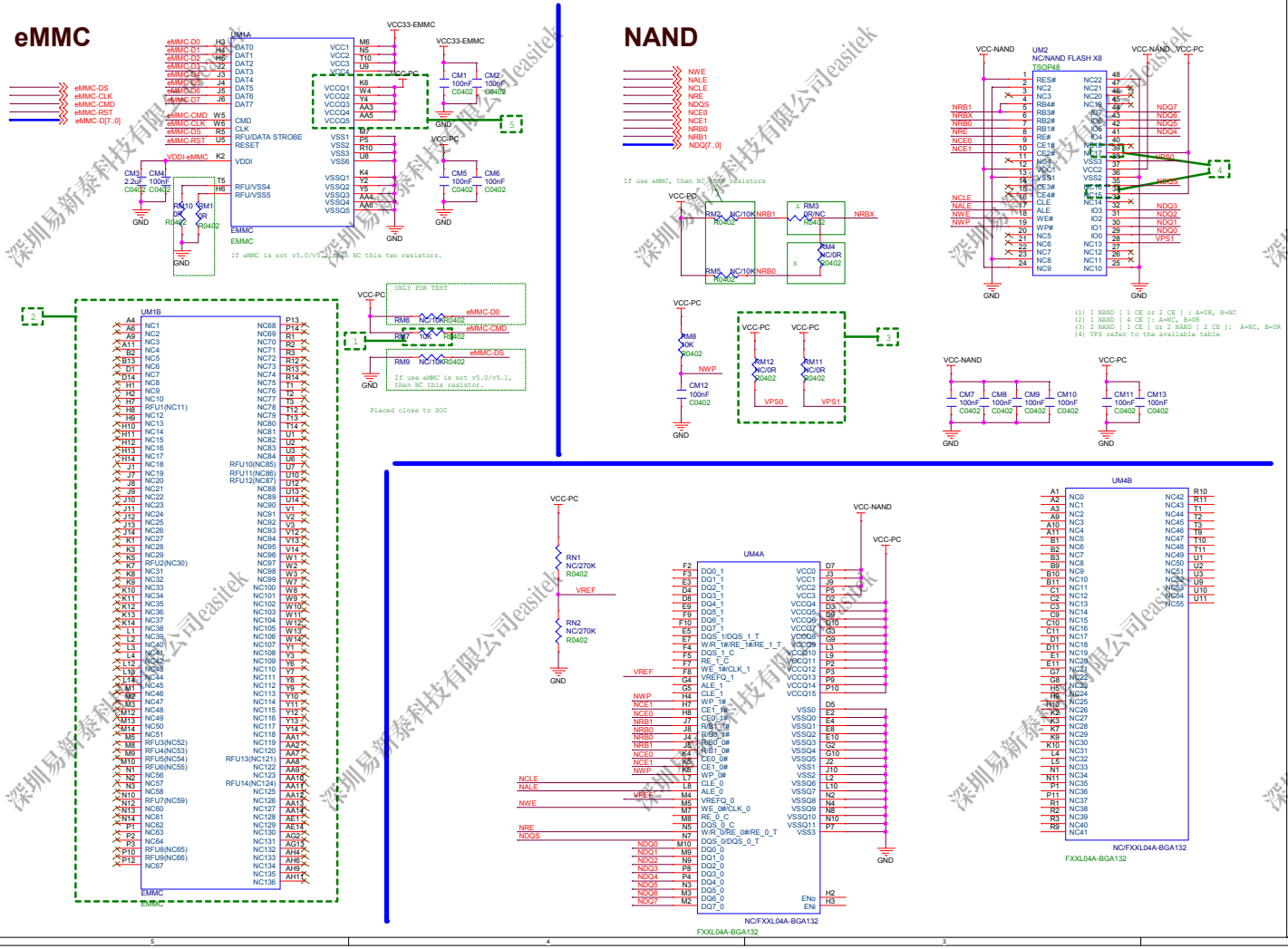


# Flash design considerations

1. CMD needs to be pulled up to VCC-PC.

2. The reserved pins, such as eMMCNC / RFU, are left unconnected. Do not connect these signals with power, ground, or other eMMC signals for easy fanout.

3. If you use Sandisk or Toshiba's nandflash, you need to pull up VPS0 and VPS1, and the other is left floating by default.

4. Some nand have 1.8V power supply, these two pins need to be connected to VCC-PC.

5. The EMMC IO power supply voltage matches the power domain voltage of the SOC GPIO.

**Important:**

*For the PCB design of the Flash module, please refer to the layout guide in the Hardware Design Guide,*
*The guide has detailed impedance, timing and crosstalk requirements;*
*Note that when EMMC and NAND are dual-layout, a daisy-chain topology is used, and EMMC is used as a routing terminal.*

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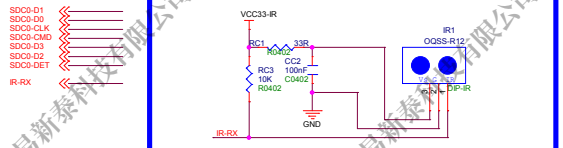
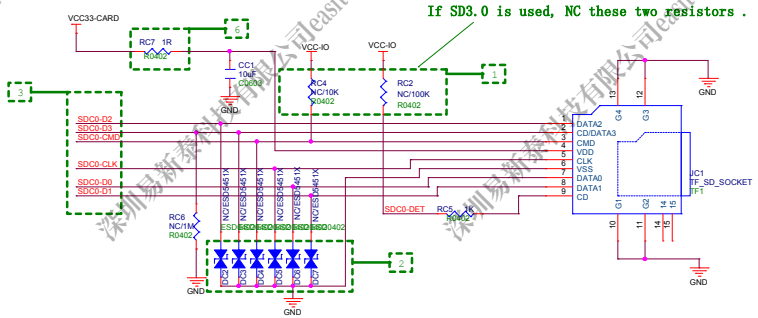
## IR

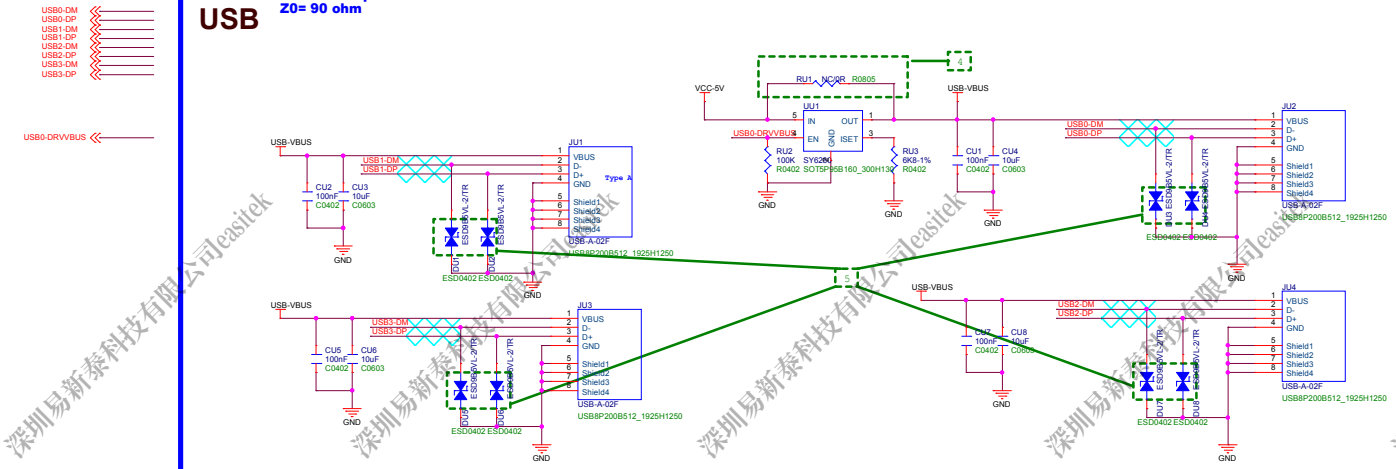



## T CARD




## USB

**Differential pairs**
**Z0= 90 ohm**




# Peripheral interface considerations-1

1. card IO supports internal 1.8V / 3.3V automatic switching, the default is 3.3V, SDCO_CMD and SDCO_DET signals have weak pull-ups internally,
External pull-ups need to be reserved to prevent insufficient internal pull-ups.

2. The parasitic capacitance of the ESD device cannot be greater than 10pF, otherwise it will affect the signal quality.

3. Please refer to the relevant guide of "Hardware Design Guide" for the design of SDIO signal layout. The guide has detailed impedance, timing and crosstalk requirements.

4. Reserve OR resistor for easy debugging.

5. USB2.0 interface signal lines USB0-DM, USB0-DP, USB1-DM, USB1-DP, USB3-DM, USB3-DP are high-speed signal lines, and connected ESD devices
Low capacitance value is required, otherwise it will affect data transmission, it is better to be less than or equal to 4pF. The USB differential signal controls the differential impedance of 90ohm and is isolated around the ground.

6. Connect a 1 ohm resistor in series to prevent the card from causing the power to drop instantly.

**Important:**

*For ESD device layout related specifications, please refer to the relevant guides in the "Hardware Design Guide" for detailed instructions.*

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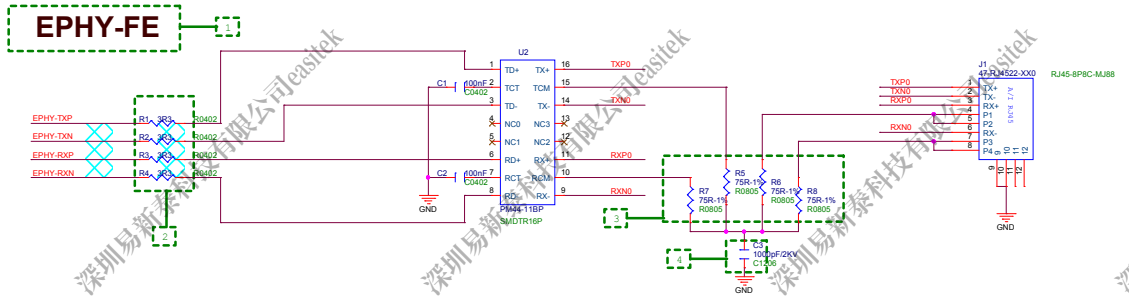


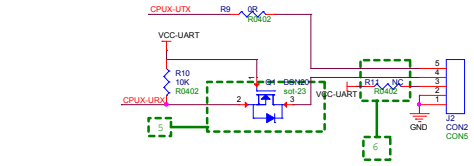


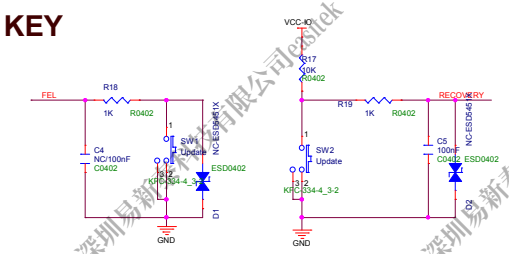


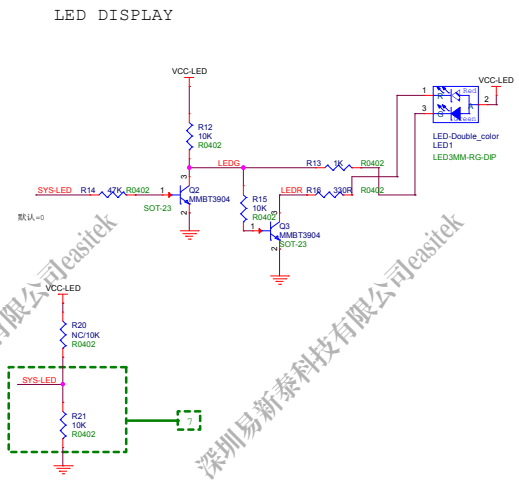


# Peripheral interface considerations-2

1. H616 internally integrates 100M EPHY, if you need to use 1000M GPHY, you need to use PI port RGMII interface and external PHY chip.

2. The resistance of the serial resistor on the Ethernet differential line should not be too large. It is recommended to reserve 0 ohms to help improve the lightning test.

3. The four 75 ohm resistors of the interface are packaged in 0805, because the small package will be burned when struck by lightning.

4. The high voltage capacitor package cannot be less than 1206, and the withstand voltage of the high voltage capacitor cannot be less than 2KV.

5. CPUX-RX needs to add MOS tube for anti-backflow design, it needs to be added in the early debugging, and can be deleted in the later mass production.

6. R11 depends on the actual serial port used for debugging, and the default is NC.

7. The SYS-LED power-on default is low, add a pull-down resistor to stabilize the level.

**Important:**

*For the differential signals of the network port and the layout of the high-voltage part, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.*

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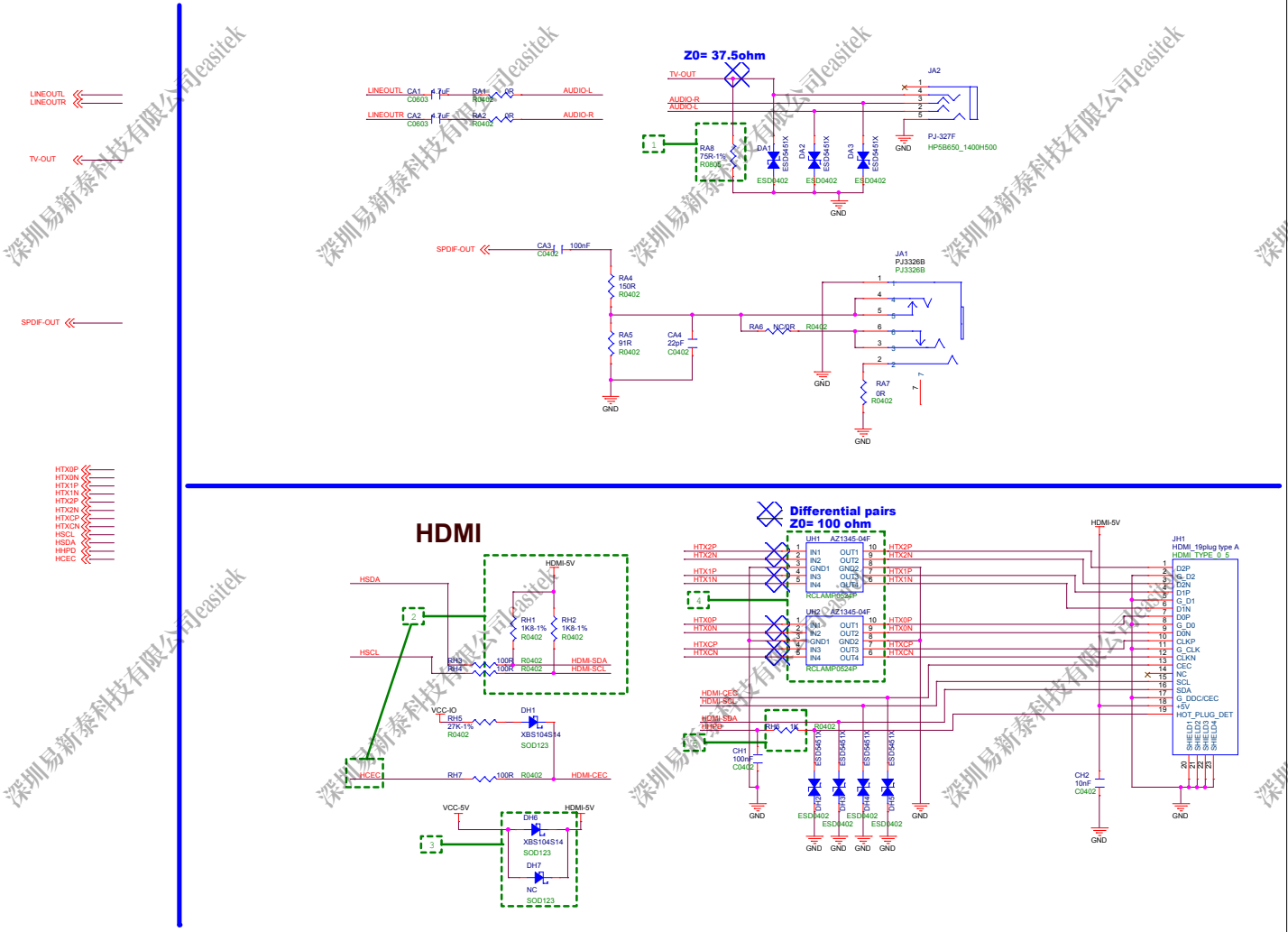


# Audio&HDMI Interface considerations

1. The 75 ohm resistor of the CVBS port needs to use the 0805 package, because the CVBS output current type, the current will flow through the resistor, if the resistor package is too small ,The resistor will be burned by heat.

2. H616 HDMI I2C and CEC have built-in levelshift circuit, which supports direct connection to device.

3. The 5V power supply of HDMI must be connected in series with Schottky diodes to prevent leakage of the TV after shutdown. The voltage drop of ordinary diodes is high, which is easy to cause HDMI power supply is lower than 4.75v, to avoid compatibility problems, please choose a Schottky diode with reduced on-voltage.

4. The dynamic resistance (Rdyn) of the ESD device used on the HDMI differential line is less than 0.35 ohms, the operating voltage is 5V, and the parasitic capacitance is less than 0.35pF,It is recommended to use AZ1345-04F.

5. HPD has a built-in levelshift circuit in H616, which can withstand 5V, so it can be directly connected in series with no voltage division.

**Important:**

*For audio and HDMI differential layout, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.*

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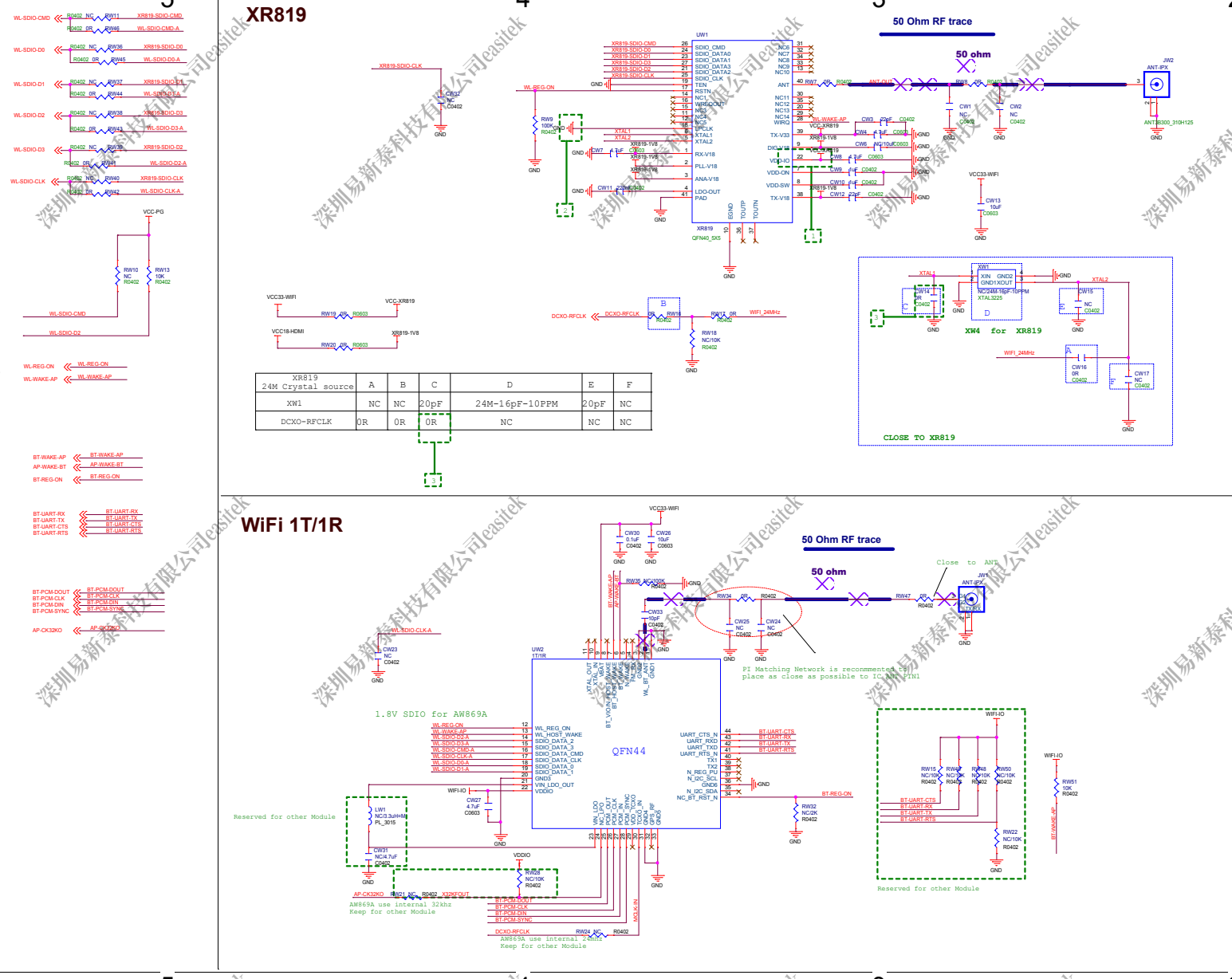


| XR819 24M Crystal source | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| XW1 | NC | NC | 20pF | 24M-16pF-10PPM | 20pF | NC |
| DCXO-RFCLK | 0R | 0R | 0R | NC | NC | NC |

# WIFI module design considerations

1. The IO power supply of WIFI is consistent with the power supply of the PG port of the SOC . Ensure that the levels of the SOC and peripherals match.

2. The 32.768K clock is provided inside XR819, and the pin is grounded.

3. When 24M Fanout is selected for crystal source, pay attention to XTAL1 grounding.

**Important:**

*For SDIO and RF antenna layout, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.*

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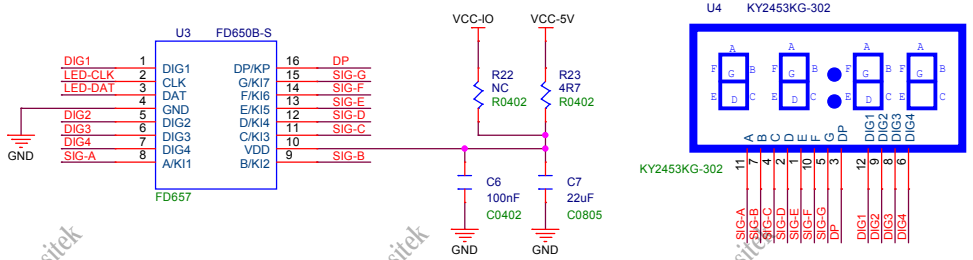
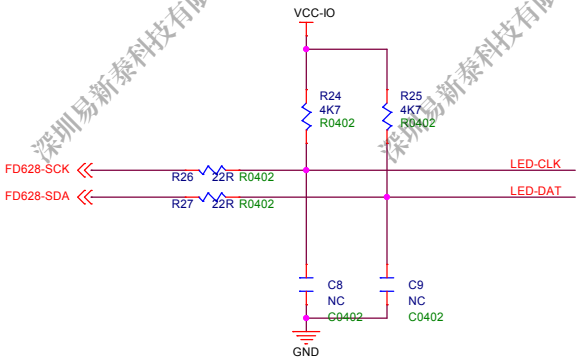
# DIGITRON

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